Access DB# 117892

SEARCH REQUEST FORM

(146)

Scientific and Technical Information Center

Requester's Full Name: Esaw Abraham Examiner #: 75692 Date: 03/24/04

Art Unit: 2133 Phone Number 305-7743 Serial Number: 09/911,634

Mail Box and Bldg/Room Location: 4B04 Results Format Preferred (circle): PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: System with Module Sharing terminations

Inventors (please provide full names): James A. McCall and Michael. W. Leddige

Earliest Priority Filing Date: 07/23/01

**For Sequence Searches Only* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

A System Comprising

- first
- second
- third
- fourth

} modules

and an error correction chip on the first, second, third fourth modules.

BEST AVAILABLE COPY

STAFF USE ONLY

Searcher: Terese Esterfield

Searcher Phone #: 308-7795

Searcher Location: 4B30

Date Searcher Picked Up: 3/29/04 4:45

Date Completed: _____

Searcher Prep & Review Time: _____

Clerical Prep Time: _____

Online Time: _____

Type of Search

NA Sequence (#): _____

AA Sequence (#): _____

Structure (#): _____

Bibliographic: _____

Litigation _____

Fulltext _____

Patent Family _____

Other _____

Vendors and cost where applicable

STN _____

Dialog _____

Questel/Orbit _____

Dr.Link _____

Lexis/Nexis _____

Sequence Systems _____

WWW/Internet _____

Other (specify) _____

PTO-1590 (8-01)

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Set     Items   Description
S1    3483476   MODULE? ? OR COMPONENT? ? OR ELEMENT? ? OR ROUTINE? ?
S2      63721   (FIRST OR 1ST OR PRIME OR PRIMARY OR INITIAL OR LEAD??? OR
             MAIN OR DOMINANT OR CARDINAL OR ORIGINAL)(2N)S1
S3      70604   (SECOND OR 2ND)(2N)S1
S4      86547   (THIRD OR 3RD)(2N)S1
S5      87504   (FOURTH OR 4TH)(2N)S1
S6     129376   ERROR()(CORRECT??? OR CONTROL) OR ECC OR FAULT()(TOLERAN? -
             OR DETECTION)
S7    1671399   CHIP? ? OR MICROCHIP OR INTEGRATED()CIRCUIT? OR IC OR RAM -
             OR RANDOM()ACCESS()MEMORY OR DRAM? OR SRAM? OR ROM? OR PROM? -
             OR EPROM? OR EEPROM? OR FLASH
S8    3639055   COUPLE? OR CONNECT? OR LINK? OR JOIN? OR UNITE?
S9     104098   STUB OR STUBS OR ROUTINE?
S10      1828   S6 (3N) S7
S11       346   S1 AND S10
S12         0   S2 AND S3 AND S4 AND S5 AND S10
S13         9   S2 AND S10
S14         1   S3 AND S10
S15         1   S4 AND S10
S16         0   S5 AND S10
S17         1   S11 AND S8 AND S9
S18     12736   S1 AND S8 AND S9
S19         1   S18 AND S10
S20        12   S13 OR S14 OR S15 OR S17 OR S19
S21        11   S20 NOT PY>2001
S22        11   S21 NOT PD>20010723
S23        10   RD (unique items)
File   8:Ei Compendex(R) 1970-2004/Mar W3
         (c) 2004 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/Feb
         (c) 2004 ProQuest Info&Learning
File 202:Info. Sci. & Tech. Abs. 1966-2004/Feb 27
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         (c) 2004 BLDSC all rts. reserv.
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         (c) 2004 Institution of Electrical Engineers
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File  94:JICST-EPlus 1985-2004/Mar W2
         (c)2004 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Feb
         (c) 2004 The HW Wilson Co.
File  95:TEME-Technology & Management 1989-2004/Mar W2
         (c) 2004 FIZ TECHNIK
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
```

23/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06298741 E.I. No: EIP03087364952
Title: Reese: A method of soft error detection in microprocessors
Author: Nickel, Joel B.; Somani, Arun K.
Corporate Source: Dept. of Elec. and Comp. Engineering Iowa State University, Ames, IA 50011, United States
Conference Title: Proceedings of the International Conference on Dependable Systems and Networks
Conference Location: Goteborg, Sweden Conference Date: 20010701-20010704
Sponsor: IEEE Computer Society (TCFTC); IFIP Working Group 10.4 on Dependable Comp. and Fault Tolerance
E.I. Conference No.: 60372
Source: Proceedings of the International Conference on Dependable Systems and Networks 2001.
Publication Year: 2001
ISBN: 0769511015
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 0302W4
Abstract: Future reliability of general-purpose processors (GPPs) is threatened by a combination of shrinking transistor size, higher clock rates, reduced supply voltages, and other factors. It is predicted that the occurrence of arbitrary transient faults, or soft errors, will dramatically increase as these trends continue. In this paper, we develop and evaluate a fault-tolerant microprocessor architecture that detects soft errors in its own data pipeline. This architecture accomplishes soft error detection through time redundancy, while requiring little execution time overhead. Our approach, called REESE (REdundant Execution using Spare **Elements**), **first** minimizes this overhead and then decreases it even further by strategically adding a small number of functional units to the pipeline. This differs from similar approaches in the past that have not addressed ways of reducing the overhead necessary to implement time redundancy in GPPs. 27 Refs.
Descriptors: Microprocessor **chips** ; Error detection; **Fault tolerant** computer systems; Computer architecture; Reliability
Identifiers: General-purpose processors (GPP)
Classification Codes:
714.2 (Semiconductor Devices & Integrated Circuits); 721.1 (Computer Theory (Includes Formal Logic, Automata Theory, Switching Theory & Programming Theory)); 722.4 (Digital Computers & Systems)
714 (Electronic Components & Tubes); 721 (Computer Circuits & Logic Elements); 722 (Computer Hardware)
71 (ELECTRONICS & COMMUNICATION ENGINEERING); 72 (COMPUTERS & DATA PROCESSING)

23/5/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05868602 E.I. No: EIP01326604107
Title: A physical design tool for built-in self-repairable RAMs
Author: Chakraborty, K.; Kulkarni, S.; Bhattacharya, M.; Mazumder, P.; Gupta, A.
Corporate Source: EDA Laboratory IBM T. J. Watson Research Center, Yorktown Heights, NY 10598, United States
Source: IEEE Transactions on Very Large Scale Integration (VLSI) Systems v 9 n 2 April 2001. p 352-364
Publication Year: 2001
CODEN: IEVSE9 ISSN: 1063-8210
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 0108W2

Abstract: In this paper, we present the description and evaluation of a novel physical design tool, BISRAMGEN, that can generate reconfigurable and **fault - tolerant RAM modules** . This tool, **first** proposed in left bracket 3 right bracket , designs a redundant RAM array with accompanying built-in self-test (BIST) and built-in self-repair (BISR) logic that can switch out faulty rows and switch in spare rows. Built-in self-repair causes significant improvement in reliability, production yield, and manufacturing cost of ASICs and microprocessors with embedded RAMs. 24 Refs.

Descriptors: *Integrated circuit layout; Computer simulation; Random access storage; Built-in self test; Logic programming; Reliability; Application specific integrated circuits; Microprocessor chips; Probability density function

Identifiers: Software Package BISRAMGEN; Built-in self repair

Classification Codes:

714.2 (Semiconductor Devices & Integrated Circuits); 723.5 (Computer Applications); 722.1 (Data Storage, Equipment & Techniques); 723.1 (Computer Programming); 922.1 (Probability Theory)

714 (Electronic Components & Tubes); 723 (Computer Software, Data Handling & Applications); 722 (Computer Hardware); 922 (Statistical Methods)

71 (ELECTRONICS & COMMUNICATION ENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

23/5/3 (Item 3 from file: 8)

05483114 E.I. No: EIP00025041693

Title: Single flux quantum one-decimal-digit RNS adder

Author: Vukovic, Nada; Feldman, Marc J.

Corporate Source: Univ of Rochester, Rochester, NY, USA

Conference Title: Proceedings of the 6th International Superconductive Electronics Conference, Part III

Conference Location: Berlin, Ger Conference Date: 19970625-19970628

E.I. Conference No.: 55750

Source: Applied Superconductivity v 6 n 10-12 Oct-Dec 1998. p 609-614

Publication Year: 1998

CODEN: ASUEE6 ISSN: 0964-1807

Language: English

Document Type: JA; (Journal Article) Treatment: A; (Applications); T; (Theoretical)

Journal Announcement: 0004W1

Abstract: Residue number system (RNS) arithmetic has a **promising** role for **fault - tolerant** high throughput superconducting single flux quantum (SFQ) circuits for digital signal processing (DSP) applications. We have designed one of the basic computational blocks used in DSP circuits, one-decimal-digit RNS adder. A new design for its **main component** , the single-modulus adder, has been developed. It combines simple and robust RSFQ elementary cells, both combinational and sequential. The central units are a circular shift register, a code converter, and the clock control circuitry. Our mod5 adder employs 195 Josephson junctions, consumes 50 mu W of power, and occupies an area of less than 2 mm**2. Chips were fabricated at HYPRES, Inc. using 1 kA/cm**2 low-T//c Niobium technology. The mod5 adder was successfully tested at low speed, and gave experimental bias margins of plus or minus 26%. (Author abstract) 13 Refs.

Descriptors: *Superconducting devices; Adders; Quantum electronics; Digital arithmetic; Fault tolerant computer systems; Digital signal processing; Cellular arrays; Shift registers; Code converters; Josephson junction devices

Identifiers: Residue number system; Single flux quantum

Classification Codes:

708.3 (Superconducting Materials); 721.3 (Computer Circuits); 931.4 (Quantum Theory); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory); 722.4 (Digital Computers & Systems); 716.1 (Information & Communication Theory)

708 (Electric & Magnetic Materials); 721 (Computer Circuits & Logic Elements); 931 (Applied Physics); 722 (Computer Hardware); 716 (Radar, Radio & TV Electronic Equipment)
70 (ELECTRICAL ENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 93 (ENGINEERING PHYSICS); 71 (ELECTRONICS & COMMUNICATIONS)

23/5/4 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05083211 E.I. No: EIP98084311436
Title: Fault tolerant CNN template design and optimization based on chip measurements
Author: Foldesy, Peter; Kek, Laszlo; Roska, Tamas; Zarandy, Akos; Bartfai, Guszti
Corporate Source: Hungarian Acad of Sciences, Budapest, Hung
Conference Title: Proceedings of the 1998 5th IEEE International Workshop on Cellular Neural Networks and Their Applications, CNNA
Conference Location: London, UK Conference Date: 19980414-19980417
Sponsor: IEEE
E.I. Conference No.: 48728
Source: Proceedings of the IEEE International Workshop on Cellular Neural Networks and their Applications 1998. IEEE, Piscataway, NJ, USA,98TH8359. p 404-409
Publication Year: 1998
CODEN: 85RZAL
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 9809W5
Abstract: This paper proposes a generic method for finding non-propagating Cellular Neural Network (CNN) templates that can be implemented reliably on a given CNN Universal Machine chip. The method has two **main components** : (i) adaptive optimization of templates based on measurements of actual CNN chips; (ii) simplification and decomposition of Boolean operators into a sequence of simpler ones that work correctly and more robustly on a given chip. Examples are presented using two concrete stored-program CNNUM chips to demonstrate the effectiveness of the proposed method, whose advantages and limitations are also discussed. (Author abstract) 18 Refs.
Descriptors: Cellular neural networks; Optimization; Microprocessor chips ; Mathematical operators; Boolean algebra; Linear **integrated circuits** ; Digital **integrated circuits** ; **Fault tolerant** computer systems
Identifiers: Cellular neural network universal machine (CNNUM) chips
Classification Codes:
723.4 (Artificial Intelligence); 921.5 (Optimization Techniques); 714.2 (Semiconductor Devices & Integrated Circuits); 921.1 (Algebra); 722.4 (Digital Computers & Systems)
723 (Computer Software); 921 (Applied Mathematics); 714 (Electronic Components); 722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS); 71 (ELECTRONICS & COMMUNICATIONS)

23/5/5 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04973160 E.I. No: EIP98034117087
Title: Dynamically reconfigurable interconnect for array processors
Author: John, Lizy Kurian; John, Eugene
Corporate Source: Univ of Texas at Austin, Austin, TX, USA
Source: IEEE Transactions on Very Large Scale Integration (VLSI) Systems v 6 n 1 Mar 1998. p 150-157
Publication Year: 1998
CODEN: IEVSE9 ISSN: 1063-8210
Language: English

Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 9805W2
Abstract: Reconfigurability of processor arrays is important due to two reasons 1) to efficiently execute different algorithms and 2) to isolate faulty processors. An array processor that is reconfigurable by the user any number of times to yield a different topology or to isolate faults is envisaged in this paper. The system has a host or controller that broadcasts a command to the interconnect to configure itself into a particular fashion. The interconnect uses static-RAM programming technology and can be programmed to different configurations by sending a different set of bits to the configuration random access memory (RAM) in the interconnect. We present three designs reconfigurable into array, ring, mesh, or Illiac mesh topologies. The first design provides no redundancy or fault tolerance. The second design is capable of graceful degradation by bypassing faulty **elements** . The **third** design is capable of graceful degradation by rerouting. The details of the interconnect and the configuration RAM contents for typical configurations are illustrated. It is seen that reconfigurable interconnect results in a highly reconfigurable or polymorphic computer. (Author abstract) 21 Refs.
Descriptors: Interconnection networks; Parallel processing systems; Random access storage; **Integrated circuit** layout; **Fault tolerant** computer systems; Algorithms
Identifiers: Polymorphic computers
Classification Codes:
722.4 (Digital Computers & Systems); 722.1 (Data Storage, Equipment & Techniques); 714.2 (Semiconductor Devices & Integrated Circuits)
721 (Computer Circuits & Logic Elements); 722 (Computer Hardware); 714 (Electronic Components); 921 (Applied Mathematics)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS); 92 (ENGINEERING MATHEMATICS)

23/5/6 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04914856 E.I. No: EIP98014027541
Title: Development of a digital terrestrial front end
Author: Mitchell, J.D.; Sadot, P.
Corporate Source: BBC Research and Development
Conference Title: Proceedings of the 1997 International Broadcasting Convention
Conference Location: Amsterdam, Neth Conference Date: 19970912-19970916
E.I. Conference No.: 47591
Source: IEE Conference Publication n 447 1997. IEE, Stevenage, Engl. p 519-524
Publication Year: 1997
CODEN: IECPB4 ISSN: 0537-9989
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications)
Journal Announcement: 9803W3
Abstract: BBC Research and Development and LSI Logic are jointly developing a front end for digital terrestrial television transmitted according to the DVB-T specification. The front end consists of two separate **components** . **First** , an analogue down-converter that converts the input signal from UHF to a low IF. Second, an integrated circuit that accepts the analogue signal from the down-converter converter and performs the required DSP operations, which include synchronisation and demodulation, to form a stream of soft decisions suitable for presentation to an FEC decoder. The development process began by agreeing a set of requirements to which the two components must conform. This paper begins by outlining these requirements. During the development of the components, many issues have been considered and resolved. A selection of the key issues and the decisions that were reached is given and, finally, a discussion of the architecture that results from these decisions is presented. (Author abstract) 4 Refs.
Descriptors: *Television transmission; Digital communication systems;

Television broadcast[illegible]g; Digital signal processing; [illegible] circuits; Synchronization; Demodulation; Error correction; Decoding; Frequency division multiplexing

Identifiers: Forward **error correction** decoder; Digital demodulation **chip** ; Quadrature amplitude modulation

Classification Codes:

716.4 (Television Systems & Equipment); 716.1 (Information & Communication Theory); 714.2 (Semiconductor Devices & Integrated Circuits); 723.2 (Data Processing)

716 (Radar, Radio & TV Electronic Equipment); 714 (Electronic Components); 723 (Computer Software)

71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING)

23/5/7 (Item 7 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

02107951 E.I. Monthly No: EIM8608-050401

Title: FAULT-TOLERANCE APPROACHES FOR VLSI/WSI ARRAYS.

Author: Negrini, Roberto; Sami, Mariagiovanna; Stefanelli, Renato

Corporate Source: Politecnico di Milano, Milan, Italy

Conference Title: Fourth Annual Computer Conference, Phoenix Conference on Computers and Communications: 1985 Conference Proceedings.

Conference Location: Scottsdale, AZ, USA Conference Date: 19850320

Sponsor: IEEE, New York, NY, USA; IEEE Computer Soc, Los Alamitos, CA, USA; IEEE Communications Soc, New York, NY, USA; IEEE, Phoenix Section, Phoenix, AZ, USA; Arizona State Univ, Tempe, AZ, USA

E.I. Conference No.: 08000

Source: Conference Proceedings - Annual Phoenix Conference 4th. Publ by IEEE, New York, NY, USA. Available from IEEE Service Cent (Cat n 85CH2154-3), Piscataway, NJ, USA p 460-468

Publication Year: 1985

CODEN: CPACE3 ISBN: 0-8186-0614-2

Language: English

Document Type: PA; (Conference Paper)

Journal Announcement: 8608

Abstract: An examination is made of the problem of dynamic reconfiguration of VLSI and WSI processing arrays; the aim is to achieve survival through reconfiguration after both production defects and faults arise during operational life. Some algorithms to solve this problem are presented and discussed by means of a formal unifying approach. Two alternative forms of redundancy are adopted: (1) structure redundancy; i. e. addition of spare processing elements to the basic array; (2) time redundancy: no spare elements are used, but working elements substitute faulty ones by performing during a multiple operation phase (throughput therefore decreases). Two different fault models are also considered: the first refers to random distribution of faults, as may happen in VLSI arrays of relatively large **elements** , while the **second** accepts clusters of faults and is more tailored to WSI arrays. 27 refs.

Descriptors: COMPUTER SYSTEMS, DIGITAL--* **Fault Tolerant** Capability; **INTEGRATED CIRCUITS** , VLSI--Redundancy

Identifiers: PROCESSING ARRAYS; STRUCTURE REDUNDANCY; TIME REDUNDANCY; RANDOM DISTRIBUTION OF FAULTS; CLUSTERS OF FAULTS

Classification Codes:

722 (Computer Hardware); 713 (Electronic Circuits); 922 (Statistical Methods)

72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS); 92 (ENGINEERING MATHEMATICS)

23/5/8 (Item 1 from file: 2)

DIALOG(R)File 2:INSPEC

01953126 INSPEC Abstract Number: B82061255

Title: ICs for Compact Disc decoders

Author(s): Matull, J.
Journal: Electronic Components & Applications vol.4, no.3 p.131-41
Publication Date: May 1982 Country of Publication: Netherlands
CODEN: ECAPD6 ISSN: 0141-6219
Language: English Document Type: Journal Paper (JP)
Treatment: General, Review (G); New Developments (N)
Abstract: Shows the **main components** of a Compact Disc audio player. The author describes the decoding section for which four new NMOS LSI circuits have been developed: SAA7010 demodulator IC (28-pin DIL); SAA7020 **error correction IC** (40-pin DIL); SAA7000 interpolation and muting IC (18-pin DIL); SAA7030 digital oversampling filter IC (24-pin DIL) used with the TDA1540 DAC (28-pin DIL) in a unique 16-bit digital-to-analogue conversion system. (2 Refs)
Subfile: B
Descriptors: field effect integrated circuits; gramophones; large scale integration; signal processing; video and audio discs
Identifiers: 16 bit D/A conversion; Compact Disc decoders; **main components** ; Compact Disc audio player; decoding section; NMOS LSI circuits ; SAA7010 demodulator IC; SAA7020 **error correction IC** ; SAA7000 interpolation and muting IC; SAA7030 digital oversampling filter IC; TDA1540 DAC
Class Codes: B2570F (Other MOS integrated circuits); B6140 (Signal processing and detection); B6450D (Audio recording media and techniques)

23/5/9 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

01899503 INSPEC Abstract Number: B82042969
Title: Component coding of the NTSC color TV signal
Author(s): Li, C.E.; Rao, K.R.
Author Affiliation: Rockwell Internat. Wescom Inc., Downers Grove, IL, USA
Conference Title: Proceedings of the Fourteenth Southeastern Symposium on System Theory p.233-6
Publisher: IEEE, New York, NY, USA
Publication Date: 1982 Country of Publication: USA x+318 pp.
Conference Date: 15-16 April 1982 Conference Location: Blacksburg, VA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: This coding involves digital demodulation of the composite signal sampled at four times the color subcarrier frequency, the implementation of the compression algorithms on the subsampled component signal, and digital reconstruction of the processed NTSC color signal. The comb filter, band pass filter, and Hilbert transformer are used for the demodulation of the luminance, saturation, and hue signals. Three different techniques DPCM, DCT, and hybrid (DCT/DPCM) coding are simulated for the data compression. The DPCM which consists of fixed two dimensional predictor, dual word length subjective quantizer, and **error correction** codes is very **promising** for the transmission of a digital TV channel over a 44.7 Mbit/s (T-3) microwave or satellite link. With the compaction capability of the DCT and intrafield hybrid coding on the subblocks of the sizes of the (8*8) luminance, (2*4) saturation, and (1*4) hue **components** , these techniques **lead** to lower bit rates for transmitting digital color video at broadcast quality. (7 Refs)
Subfile: B
Descriptors: colour television; data compression; encoding; video signals
Identifiers: 44.7 Mbit/s microwave link; luminance signal; saturation signal; component coding; NTSC color TV signal; digital demodulation; compression algorithms; comb filter; band pass filter; Hilbert transformer; hue signals; DPCM; DCT; data compression; two dimensional predictor; dual word length subjective quantizer; error correction codes; digital TV channel; satellite link; hybrid coding
Class Codes: B6120B (Codes); B6140 (Signal processing and detection); B6430 (Television equipment, systems and applications)

23/5/10 (Item 1 from file: 233)
DIALOG(R)File 233:Internet & Personal Comp. Abs.

00099241 84DD12-011

Readers pitch M68000

Duncan, Ray

Dr. Dobb's Journal , Dec 1984 , v9 n12 p88-94, 5 Pages
ISSN: 0278-6508
Languages: English
Document Type: Column

machine language program .

Geographic Location: **United** States

16-BIT SOFTWARE TOOLBOX column discusses the difficulty of developing software for the Motorola 68000 microcprocessor, presents patches for the 8086 microprocessor, reviews features of the new 80286 and its instruction set and mentions an error correction for an 8086 assembly instruction **routine** published in the June 1984 issue.

Descriptors: **Integrated Circuits** ; Debugging; **Error Correction** ; Hardware Evaluation; 68000; 8086; 80286

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Set     Items   Description
S1      20797   MODULE? ? OR COMPONENT? ? OR ELEMENT? ? OR ROUTINE? ?
S2        394   (FIRST OR 1ST OR PRIME OR PRIMARY OR INITIAL OR LEAD??? OR
              MAIN OR DOMINANT OR CARDINAL OR ORIGINAL)(2N)S1
S3         25   (SECOND OR 2ND)(2N)S1
S4         95   (THIRD OR 3RD)(2N)S1
S5          9   (FOURTH OR 4TH)(2N)S1
S6       1097   ERROR()(CORRECT??? OR CONTROL) OR ECC OR FAULT()(TOLERAN? -
              OR DETECTION)
S7      13575   CHIP? ? OR MICROCHIP OR INTEGRATED()CIRCUIT? OR IC OR RAM -
              OR RANDOM()ACCESS()MEMORY OR DRAM? OR SRAM? OR ROM? OR PROM? -
              OR EPROM? OR EEPROM? OR FLASH
S8      26286   COUPLE? OR CONNECT? OR LINK? OR JOIN? OR UNITE?
S9       1185   STUB OR STUBS OR ROUTINE?
S10         2   S6 (3N) S7
S11         0   S1 AND S10
S12         0   S2 AND S10
S13       256   S8 AND S1 AND S9
S14         2   S13 AND (LOOP OR LOOPS)
S15         2   S14 NOT PY>2001
S16         2   S15 NOT PD>20010723
S17         4   S13 AND S6
S18         4   S17 NOT S16
S19         4   S18 NOT PY>2001
S20         4   S19 NOT PD>20010723
File 256:SoftBase:Reviews,Companies&Prods. 82-2004/Feb
         (c)2004 Info.Sources Inc
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20/5/1
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

01605441 DOCUMENT TYPE: Product

PRODUCT NAME: SiteNet SNMP Manager (605441)

Liebert Corp (544591)
1050 Dearborn Dr
Columbus, OH 43229 United States
TELEPHONE: (614) 888-0246

RECORD TYPE: Directory

CONTACT: Sales Department

SiteNet SNMP Manager is a series of snap-in screens for network management systems that seamlessly incorporates any Liebert uninterruptible power supply (UPS) with existing management software and provides user-friendly monitoring and control of power. Network power management features of SiteNet SNMP Manager include complete network power information in a graphic format, instead of a text-only MIB interface; alarms and on-screen messages; pull-down menus and a toolbar for fast access to all program capabilities; and an auto-discovery feature that immediately identifies and labels all Liebert UPS systems on a network. When power problems do happen, SiteNet SNMP Manager offers the following options: staged shutdown of **connected** equipment to reserve battery power for mission-critical servers and other vital nodes; start-up and transfer of power to auxiliary generators; and selecting and running of multiple, pre-set **routines** based on actual conditions. SiteNet SNMP Manager is compatible with the network manager HP OpenView.

DESCRIPTORS: **Fault Tolerance** ; Network Administration; Network Management; Network Software; Performance Monitors; System Monitoring; System Performance

HARDWARE: HP; IBM PC & Compatibles; Sun; UNIX
OPERATING SYSTEM: AIX; HP-UX; Solaris; Windows; Windows NT/2000; Windows XP
PROGRAM LANGUAGES: Not Available
TYPE OF PRODUCT: Mini; Micro; Workstation
POTENTIAL USERS: Cross Industry, Network Administrators
PRICE: Available upon request

SERVICES AVAILABLE: Warranty; hardware sales
REVISION DATE: 20030804

20/5/2
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

01020311 DOCUMENT TYPE: Product

PRODUCT NAME: MopUPS (020311)

Oneac Corp (544604)
27944 N Bradley Rd
Libertyville, IL 60048 United States
TELEPHONE: (847) 816-6000

RECORD TYPE: Directory

CONTACT: Sales Department

Oneac's MopUPS monitors ONEAC UPSes to automatically shut a system down should a prolonged AC failure occur. For remote notification of threats to system uptime, MopUPS provides UPS fault messaging through pager, e-mail, network, or SNMP traps for UPSs **connected** to workstations. When a shutdown occurs, MopUPS allows network access for troubleshooting. Users can reach current conditions, event and data log files, and UPS configuration options via a remote workstation or server. Administrators can also schedule **routine** shutdowns using MopUPS, which facilitates system tuning or upgrades during periods of low use. MopUPS helps users shut down voice or data networks, and it does not require manual intervention.

DESCRIPTORS: **Fault Tolerance** ; LANs; Network Administration; Network Software; System Monitoring; Telecommunications; WANs

HARDWARE: EtherNet; IBM PC & Compatibles; UNIX
OPERATING SYSTEM: NetWare; UNIX; Windows; Windows NT/2000
PROGRAM LANGUAGES: Not Available
TYPE OF PRODUCT: Mainframe; Mini; Micro; Workstation
POTENTIAL USERS: Network Administrators of Voice and Data Networks
PRICE: Available upon request

REVISION DATE: 20010130

20/5/3

00118056 DOCUMENT TYPE: Review

PRODUCT NAMES: Cobalt NASRaQ (763641)

TITLE: Good things come in small packages
AUTHOR: Baltazar, Henry
SOURCE: PC Week, v16 n28 p78(1) Jul 12, 1999
ISSN: 0740-1604

RECORD TYPE: Review
REVIEW TYPE: Review
GRADE: B

Cobalt Networks' Cobalt NASRaq device, a stackable network storage device, gets good marks overall, with excellent usability. It maximizes the use of computer room floorspace by providing a storage capacity of 32GB in a device only 2 inches high. Installation and management are easy, and a front panel LCD screen and control buttons show device status and permit quick changes to network settings. The two-disk unit is suitable only for remote office or workgroup usage. A small form factor resets the bar for NAS devices, and Web-enabled administration, and setup wizards streamline installation and management. Administrators can set storage quotas for users, and a 50-pin Ultra SCSI port is included for peripheral **connection** . The unit has to be rebooted to change basic settings, and SCSI peripherals have to be configured manually via telnet. Testers had the device set up in under a half hour, with the lion's share of configuration time spent on RAID 1 disk mirroring setup. The setup **routine** permitted testers to activate Server Message Block, AppleShare, and Network File System protocols to provide file services to many clients. Cobalt NASRaq can use Windows NT domains for authentication control, but testers were also able to store user account information locally. Cobalt NASRaq runs Linux 2.0, which does not support scalable SMP networking, but only a single 64-bit 250MHz MIPS processor is used. Web administration utilities use an Apache 1.3.3 World Wide Web server.

PRICE: $2799

COMPANY NAME: Sun Microsystems Inc (665622)

SPECIAL FEATURE: Charts
DESCRIPTORS: **Fault Tolerance** ; IBM PC & Compatibles; LANs; Linux; Network Administration; Network Software; Storage Management; Windows NT/2000
REVISION DATE: 20020630

20/5/4
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

00111955 DOCUMENT TYPE: Review

PRODUCT NAMES: Microsoft Windows 3.1 (740896); Microsoft Windows NT (347973); MacOS X Server (725896); Digital UNIX (555835)

TITLE: Heart of OS being pulled in different directions
AUTHOR: Hayes, Frank
SOURCE: Computerworld, v32 n45 p28(1) Nov 9, 1998
ISSN: 0010-4841
HOMEPAGE: http://www.computerworld.com

RECORD TYPE: Review
REVIEW TYPE: Product Analysis
GRADE: Product Analysis, No Rating

Microsoft's Microsoft Windows 3.1 and Microsoft Windows NT both have large operating system (OS) kernels, while Apple Computer's Mac OS Server and Compaq's Digital UNIX have a microkernel. A conventional kernel provides all functions for applications; it manages memory and files, **links** applications to I/O devices, and apportions processor time. The traditional kernel also supports security and **fault tolerance** , or automatic recovery when portions of the system fail. All parts of the kernel run in kernel mode, and all have access to system data and hardware. Applications run in user mode, so that applications have access to their own sections of memory. Applications use kernel functions through application programming interfaces (APIs), or a set of standard **routines** used by programs. Microsoft has added a database and UNIX APIs to the Windows NT kernel, a reflection of the trend toward more functionality in kernels. However, Sun, DEC, and Apple are trying out a new OS design that uses a microkernel. With a microkernel, only a few key functions, including division of memory and processor time among applications and communications between software processes, operate in kernel mode. All other functions run as applications, including file systems, networking, and device drivers. Microkernels are appropriate for massively parallel systems, but performance can slow, since file systems and device drivers cannot gain direct access to all system data required by an application.

COMPANY NAME: Microsoft Corp (112127); Apple Computer Inc (114936); Compaq Computer Corp (462977)
SPECIAL FEATURE: Charts Tables
DESCRIPTORS: Apple Macintosh; IBM PC & Compatibles; MacOS; Memory Management; Network Servers; Network Software; Operating Systems; Parallel Processing; UNIX; Windows
REVISION DATE: 20020819

```
Set     Items   Description
S1    3805802   MODULE? ? OR COMPONENT? ? OR ELEMENT? ? OR ROUTINE? ?
S2     158388   (FIRST OR 1ST OR PRIME OR PRIMARY OR INITIAL OR LEAD??? OR
              MAIN OR DOMINANT OR CARDINAL OR ORIGINAL)(2N)S1
S3      63191   (SECOND OR 2ND)(2N)S1
S4      11420   (THIRD OR 3RD)(2N)S1
S5       2924   (FOURTH OR 4TH)(2N)S1
S6      33354   ERROR()(CORRECT??? OR CONTROL) OR ECC OR FAULT()(TOLERAN? -
              OR DETECTION)
S7    1031441   CHIP? ? OR MICROCHIP OR INTEGRATED()CIRCUIT? OR IC OR RAM -
              OR RANDOM()ACCESS()MEMORY OR DRAM? OR SRAM? OR ROM? OR PROM? -
              OR EPROM? OR EEPROM? OR FLASH
S8    4651947   COUPLE? OR CONNECT? OR LINK? OR JOIN? OR UNITE?
S9      35633   STUB OR STUBS OR ROUTINE?
S10       540   S6 (3N) S7
S11       120   S1 AND S10
S12         9   S11 AND IC=H03M?
S13         8   S11 AND MC=(T01-H01B3 OR U11-D03C1A OR U14-A10)
S14        16   S12 OR S13
S15         0   S2 AND S3 AND S4 AND S5 AND S10
S16         3   S2 AND S10
S17         3   S3 AND S10
S18         1   S4 AND S10
S19         0   S5 AND S10
S20      7096   S8 AND S1 AND S9
S21       134   S20 AND (LOOP OR LOOPS)
S22       138   S16 OR S17 OR S18 OR S21
S23         2   S22 AND IC=H03M?
S24         3   S22 AND MC=(T01-H01B3 OR U11-D03C1A OR U14-A10)
S25        18   S14 OR S23 OR S24
File 347:JAPIO Nov 1976-2003/Nov(Updated 040308)
        (c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200419
        (c) 2004  Thomson Derwent
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25/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06057447 **Image available**
DIGITAL SIGNAL PROCESSOR AND ITS METHOD

PUB. NO.: 10-340547 [JP 10340547 A]
PUBLISHED: December 22, 1998 (19981222)
INVENTOR(s): KAWAHARA MINORU
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-148205 [JP 97148205]
FILED: June 05, 1997 (19970605)
INTL CLASS: [6] G11B-020/18; G11B-020/18; G11B-020/18; G11B-020/14; **H03M-013/00**
JAPIO CLASS: 42.5 (ELECTRONICS -- Equipment); 42.4 (ELECTRONICS -- Basic Circuits)
JAPIO KEYWORD: R098 (ELECTRONIC MATERIALS -- Charge Transfer **Elements** , CCD & BBD); R101 (APPLIED ELECTRONICS -- Video Tape Recorders, VTR); R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers

ABSTRACT

PROBLEM TO BE SOLVED: To properly perform ID reproduction in an ECC(**error correction** code) decoder **IC** .

SOLUTION: A synchronous pattern is detected from a data packet. Judgment is made whether or not the synchronous pattern is correct, a flag FabSync is provided at the head of the packet on the basis of the judgment result. In the case of ID reproduction that is carried out after the correction of an internal code, this flag is referred to. If the oneself is usable, an ID0 is used as it is (S1). If inertia is usable and if no error is present at the head of the packet on the basis of the FabSync, the ID is reproduced by the inertia (S3). When NG is at S3, ID reproduction is performed by going upstream (S5, S7). If the situation can not use the going upstream, the inertia is used. When NG is at S9, pid0 which is the ID estimated from the timing of head switching is used as ID0

25/5/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015403919 **Image available**
WPI Acc No: 2003-466059/200344
Related WPI Acc No: 2003-289064; 2003-330843; 2003-341550
XRPX Acc No: N03-370713
Semiconductor chip module connection **system has two groups of conductor paths each having short** loop **through section which** couples **with** modules **through** stubs
Patent Assignee: LEDDIGE M W (LEDD-I); MCCALL J A (MCCA-I)
Inventor: LEDDIGE M W; MCCALL J A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030018940	A1	20030123	US 2001911634	A	20010723	200344	B

Priority Applications (No Type Date): US 2001911634 A 20010723
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030018940	A1		37	H03M-013/00	

Abstract (Basic): US 20030018940 A1
NOVELTY - Two group of conductor paths extend from the circuit board (12) comprising several **connectors** (20,22), to the semiconductor chip **modules** . Each group has a short **loop** through

section which **couples** with the **modules** through **stubs** .
USE - For **connecting** semiconductor chip **modules** such as single inline memory **modules** (SIMMs), dual inline memory **modules** (DIMMs) used in SDRAM.
ADVANTAGE - Reduces the number of **connectors** .
DESCRIPTION OF DRAWING(S) - The figure shows the schematic plan view of the circuit board.
circuit board (12)
connectors (20,22)
pp; 37 DwgNo 2/39
Title Terms: SEMICONDUCTOR; CHIP; **MODULE** ; **CONNECT** ; SYSTEM; TWO; GROUP; CONDUCTOR; PATH; SHORT; **LOOP** ; THROUGH; SECTION; **COUPLE** ; **MODULE** ; THROUGH; **STUB**
Derwent Class: T01; U11; U14
International Patent Class (Main): **H03M-013/00**
File Segment: EPI

25/5/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015362428 **Image available**
WPI Acc No: 2003-423366/200340
XRPX Acc No: N03-338028
Active termination resistor control method in DRAM system includes a switching circuit to selectively output a synchronous or asynchronous input buffer according to an operation mode
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU); KYUNG K (KYUN-I)
Inventor: KYUNG K; KYUNG G H
Number of Countries: 034 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1306849	A2	20030502	EP 2002257252	A	20021018	200340 B
US 20030099138	A1	20030529	US 2001330083	P	20011019	200346
			US 2002224632	A	20020821	
KR 2003032831	A	20030426	KR 200248708	A	20020817	200354
CN 1417805	A	20030514	CN 2002157515	A	20021019	200355
JP 2003223784	A	20030808	JP 2002305034	A	20021018	200361
US 20040032319	A1	20040219	US 2003377604	A	20030304	200414

Priority Applications (No Type Date): US 2002224632 A 20020821; KR 200164777 A 20011019; KR 200248708 A 20020817; US 2001330083 P 20011019
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1306849	A2	E	36	G11C-007/10	
Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR					
US 20030099138	A1		23	G11C-007/00	Provisional application US 2001330083
KR 2003032831	A			G11C-011/4093	
CN 1417805	A			G11C-011/4063	
JP 2003223784	A		19	G11C-011/401	
US 20040032319	A1			H03M-001/80	

Abstract (Basic): EP 1306849 A2
NOVELTY - A control device and method controlling an on/off state of the active termination resistors (431,432) of a DRAMs (460,470,480,490) irrespective of an operation mode of DRAMs mounted in a single or dual in-line memory **module** . A buffer circuit is mounted in a memory circuit that includes synchronous buffer and asynchronous buffer inputs **coupled** to the signal terminal, and a switching circuit to output either the synchronous or asynchronous input buffer according to an operation mode of the memory circuit.
DETAILED DESCRIPTION - The memory system 400 includes a chipset, a data bus 420, a first memory **module** 440 in which DRAMs 460 and 470 are mounted, and a second memory **module** 450 in which DRAMs 480 and

490 are mounted. The memory **modules** may be mounted in card slots (not shown) of the memory system.

The first and second memory **modules** 440 and 450 may be implemented, for example, by a dual in-line memory **module** (DIMM) or single in-line memory **module** (SIMM). Also, each of the chipset 410 and the DRAMs 460, 470, 480 and 490 are equipped with a driver and an input buffers for the writing and reading of data.

The chipset includes an active terminator 430 which is enabled and disabled by an ATCChipSet (ATCCS) signal. In addition, each of the DRAMs include active terminator resistors 432 which are enabled and disabled by the ATC0 and ATC1 signals. Further, the chipset includes an ATC signal generator 411 which generates a chipset control signal ATCCS, a first control signal ATC0, and a second control signal ATC1 according to read/write modes of the memory **modules** . When data is written to or read from the DRAMs 460 and 470, the chipset 410 outputs a data write/read command to the DRAMs 460 and 470 mounted in the first memory **module** 440. In addition, the chipset outputs the first control signal ATC0 to the DRAMs 460 and 470 for disabling the active terminator 431 of the DRAMs 460 and 470, and outputs the second control signal ATC1 to the DRAMs 480 and 490 for enabling the active terminators 432 of the DRAMs 480 and 490. Each of the DRAMs include a synchronization circuit, e.g. a delay lock **loop** (DLL) or phase locked **loop** (PLL), for generating an internal clock in synchronization with an external clock.

USE - Devices and methods of controlling active termination resistors which are used to improve signaling characteristics in DRAM memory circuits and systems.

ADVANTAGE - The invention asynchronously or synchronously controls the active terminator resistors according to an operational mode i.e. active, power-down and standby modes of each memory **module** to improve the signaling characteristics.

DESCRIPTION OF DRAWING(S) - The drawing figure shows a memory system having an active termination **stub** bus configuration.

Memory system (400)
Data bus (420)
Active termination resistors (431,432)
Memory **modules** (440,450)
Dynamic Random Access Memories (460,470,480,490)
ATCChipSet signal (ATCCS)
pp; 36 DwgNo 4/21

Title Terms: ACTIVE; TERMINATE; RESISTOR; CONTROL; METHOD; DRAM; SYSTEM; SWITCH; CIRCUIT; SELECT; OUTPUT; SYNCHRONOUS; ASYNCHRONOUS; INPUT; BUFFER ; ACCORD; OPERATE; MODE
Derwent Class: U13; U14; U21; U25
International Patent Class (Main): G11C-007/00; G11C-007/10; G11C-011/401; G11C-011/4063; G11C-011/4093; **H03M-001/80**
International Patent Class (Additional): G06F-012/00; G06F-013/16; G11C-005/00; H03K-017/687; H03K-019/0175
File Segment: EPI

25/5/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015138098 **Image available**
WPI Acc No: 2003-198624/200319
XRPX Acc No: N03-157846

Multipurpose error-control code construction method for e.g. DRAM , **involves substituting** error control **code matrix** elements **with isometric** elements **of finite** element **fields using biunique correspondences between isometric** elements

Patent Assignee: STMICROELECTRONICS SRL (SGSA)
Inventor: FERRARI P; GREGORI S; TORELLI G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week

US 20020157059 A1 20021024 US 200115949 A 2001[redacted]02 200319 B

Priority Applications (No Type Date): IT 2000TO1049 A 20001107
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20020157059 A1 18 H03M-013/00

Abstract (Basic): US 20020157059 A1
NOVELTY - The design specifications of an error-control code are acquired. The minimum value of n, maximum values of n and k are calculated for generating a matrix of the error control code on finite **element** fields. Binary polynomial representations of the fields are constructed to identify isomeric **elements** of the fields, which are substituted in each of the matrix **elements** using biunique correspondences between the isomeric **elements** .
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(1) Multi-purpose error control method; and
(2) Computer storage device.
USE - For constructing multi-purpose error-control code for multi-level semiconductor memories such as volatile memory e.g. Dynamic Random Access Memory (DRAM) and non-volatile memory e.g. Electrically Erasable Programmable Read Only Memory (EEPROM) and flash memory.
ADVANTAGE - By substituting the error control code matrix **elements** with the isomeric **elements** using the biunique correspondences between the isomeric **elements** , errors in the memory cells are efficiently controlled, hence reliability in every operating mode and exploitation of memory cells used for the control are improved, additional area required for the memory and additional delay time are reduced.
DESCRIPTION OF DRAWING(S) - The figure shows the flowchart illustrating the multi-purpose error-control code construction process.

pp; 18 DwgNo 6/8
Title Terms: MULTIPURPOSE; ERROR; CONTROL; CODE; CONSTRUCTION; METHOD; DRAM ; SUBSTITUTE; ERROR; CONTROL; CODE; MATRIX; **ELEMENT** ; ISOMETRIC; **ELEMENT** ; FINITE; **ELEMENT** ; FIELD; ISOMETRIC; **ELEMENT**
Derwent Class: T01; U14; U21
International Patent Class (Main): **H03M-013/00**
File Segment: EPI

25/5/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014826065 **Image available**
WPI Acc No: 2002-646771/200270
XRPX Acc No: N02-511512
Chip kill method for low end server, involves executing double word operation to continuous memory location in single DIMM module
Patent Assignee: HEWLETT-PACKARD CO (HEWP)
Inventor: RAYNHAM M B
Number of Countries: 002 Number of Patents: 002
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
JP 2001142789 A 20010525 JP 2000320318 A 20001020 200270 B
US 6493843 B1 20021210 US 99429749 A 19991028 200301

Priority Applications (No Type Date): US 99429749 A 19991028
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
JP 2001142789 A 10 G06F-012/16
US 6493843 B1 G11C-029/00

Abstract (Basic): JP 2001142789 A
NOVELTY - The chip kill operation is executed by executing double

word operation to continuous memory locations in single DIMM **module** in the low end system in which the required number of **error correction** bits for executing **chip** kill operation is not specified.

USE - For low end server or work station.

ADVANTAGE - Provides memory configuration for installing kill error detecting function on low end server without requiring non-standard **component** and additional memory.

DESCRIPTION OF DRAWING(S) - The figure depicts a flowchart illustrating the chip kill operation. (Drawing includes non-English language text).

pp; 10 DwgNo 1/1

Title Terms: CHIP; KILL; METHOD; LOW; END; SERVE; EXECUTE; DOUBLE; WORD; OPERATE; CONTINUOUS; MEMORY; LOCATE; SINGLE; **MODULE**

Derwent Class: T01; U21

International Patent Class (Main): G06F-012/16; G11C-029/00

International Patent Class (Additional): G06F-011/10; **H03M-013/00**

File Segment: EPI

25/5/6 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014736061 **Image available**

WPI Acc No: 2002-556765/200259

XRPX Acc No: N02-440682

Hierarchically configured dirty random access memory **used in** fault tolerant **computer system, stores specific dirty bit indicator which is set as higher level indicator based on state of respective pages of memory**

Patent Assignee: SUN MICROSYSTEMS INC (SUNM); GARNETT P J (GARN-I); HARRIS J G (HARR-I)

Inventor: GARNETT P J; HARRIS J G

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020065985	A1	20020530	US 2001938808	A	20010824	200259	B
GB 2369694	A	20020605	GB 200029108	A	20001129	200259	
GB 2369694	B	20021016	GB 200029108	A	20001129	200276	

Priority Applications (No Type Date): GB 200029108 A 20001129

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020065985	A1		29	G06F-013/00	
GB 2369694	A			G06F-011/16	
GB 2369694	B			G06F-011/16	

Abstract (Basic): US 20020065985 A1

NOVELTY - A dirty memory stores dirty bit indicators corresponding to different pages of the memory. A specific dirty group indicator is set as higher level indicator based on state of respective pages of the memory.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Computer system; and

(2) Equivalent memory state reinstatement management method.

USE - Used in fault tolerant computer system.

ADVANTAGE - Enables to identify specific **components** of a **main** memory which is to be copied, thereby avoids copying of whole contents of memory, which increases processing speed. The required portions of another level memory are identified using previous level memory. Increases accessing speed by using several levels of indicator. Prevents alteration of memory content by inhibiting direct memory access by input/output devices. Prevents further dirtying to permit a final cycle of copying any page of memory which is dirtied from a processing set to the other.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic overview

of the fault tolerant system.
pp; 29 DwgNo 1/17
Title Terms: HIERARCHY; CONFIGURATION; DIRT; RANDOM; ACCESS; MEMORY; FAULT; TOLERATE; COMPUTER; SYSTEM; STORAGE; SPECIFIC; DIRT; BIT; INDICATE; SET; HIGH; LEVEL; INDICATE; BASED; STATE; RESPECTIVE; PAGE; MEMORY
Derwent Class: T01
International Patent Class (Main): G06F-011/16; G06F-013/00
File Segment: EPI

25/5/7 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014660136 **Image available**
WPI Acc No: 2002-480840/200252
XRPX Acc No: N02-379759
Memory module **system for use as DRAM, has first and** second module **cards with** DRAM components **and** ECC element **to be plugged into first and second plug-in bases in a coordinated manner**
Patent Assignee: INFINEON TECHNOLOGIES AG (INFN)
Inventor: ROEHR T
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 10050702	A1	20020425	DE 1050702	A	20001013	200252	B

Priority Applications (No Type Date): DE 1050702 A 20001013
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 10050702	A1		7	G11C-007/00	

Abstract (Basic): DE 10050702 A1
NOVELTY - A memory **module** system has a **first module** card (1) with DRAM **components** (2) and an ECC **element** (3). A **second module** card also has DRAM **components** . The **first module** card is plugged into a first plug-in base and the **second module** card into a second plug-in base. A sentinel flag **element** (7) ensures definite coordination of **module** cards and plug-in bases.
USE - In advanced DRAM technology with 64-bit data bus widths.
ADVANTAGE - The sentinel flag **element** makes definite mechanical coordination possible between the **first** and **second module** cards and the first and second plug-in bases.
DESCRIPTION OF DRAWING(S) - The drawing shows an operating version of the present invention with two **module** cards with or without error recognition.
First module card (1)
DRAM **component** (2)
ECC **element** (3)
Sentinel flag **element** (7)
pp; 7 DwgNo 4A/10
Title Terms: MEMORY; **MODULE** ; SYSTEM; DRAM; FIRST; SECOND; **MODULE** ; CARD; DRAM; **COMPONENT** ; ECC; **ELEMENT** ; PLUG; FIRST; SECOND; PLUG; BASE; COORDINATE; MANNER
Derwent Class: T01; U11; U13; U14; V04
International Patent Class (Main): G11C-007/00
International Patent Class (Additional): G06F-012/00; H01R-013/64
File Segment: EPI

25/5/8 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014462581 **Image available**
WPI Acc No: 2002-283284/200233
XRPX Acc No: N02-221347

Error detection and correction method for data processing system, involves transmitting parity bits and corresponding data bits and testing correspondence between received parity bits and data bits

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: MACIVER M A
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2361848	A	20011031	GB 20009804	A	20000425	200233	B
US 20020013929	A1	20020131	US 2001838074	A	20010419	200233	

Priority Applications (No Type Date): GB 20009804 A 20000425
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2361848	A		21	G06F-011/10	
US 20020013929	A1			G06F-011/00	

Abstract (Basic): GB 2361848 A

NOVELTY - The parity bits corresponding to the entire stream of data bits contained in an interface (208) are generated in transmitter (202). The parity and data bits are transmitted across the interface. A parity checker (212) is included in a receiver (210) to test the correspondence of the parity bits with the data bits. The errors in the data bits for which parity is encoded, are detected and corrected.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for system for error detection and correction in an interface between two portions of the data processing system.

USE - For detecting and correcting errors in an interface between sending and receiving **elements** of data processing system such as computer servers, personal computers. For carrying out **error correction** of a **chip** , package, card or system level.

ADVANTAGE - Susceptibility to hard faults and to intermittent faults is reduced by testing the correspondence between received parity bits and data bits. System availability is increased due to the ability to detect and correct errors in data transmission.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of error detection and correction system.

Transmitter (202)
Interface (208)
Receiver (210)
Parity checker (212)

pp; 21 DwgNo 2/5

Title Terms: ERROR; DETECT; CORRECT; METHOD; DATA; PROCESS; SYSTEM; TRANSMIT; PARITY; BIT; CORRESPOND; DATA; BIT; TEST; CORRESPOND; RECEIVE; PARITY; BIT; DATA; BIT
Derwent Class: T01; U21
International Patent Class (Main): G06F-011/00; G06F-011/10
International Patent Class (Additional): **H03M-013/19**
File Segment: EPI

25/5/9 (Item 8 from file: 350)

014442005 **Image available**
WPI Acc No: 2002-262708/200231
XRPX Acc No: N02-204225

Flash memory circuit judges whether inspection data and data are read-out simultaneously and whether any error is in read-out data, based on which error correction circuit is controlled

Patent Assignee: NIPPONDENSO CO LTD (NPDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001337866	A	20011207	JP 2000156903	A	20000526	200231	B

Priority Applications (No Type Date): JP 2000156903 A 20000526
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
JP 2001337866 A 6 G06F-012/16

Abstract (Basic): JP 2001337866 A
NOVELTY - A CPU reads out inspection data and data stored in a flash memory (2) through data-bus of 16-bit size. An access controller comprised by latches (6U,6L), buffers (5U,5L) and a control unit, judges whether data and inspection data are read-out simultaneously and whether any error is in the read-out data. Based on the judgment result, an error correction circuit corrects the error.
USE - **Flash** memory circuit with **error correction** control function.
ADVANTAGE - Improves reliability and avoids influence on capacity of memory circuit, due to inclusion of error correction circuit.
DESCRIPTION OF DRAWING(S) - The figure shows the functional block diagram of the electric **component** of a memory circuit. (Drawing includes non-English language text).
Flash memory (2)
Buffers (5U,5L)
Latches (6U,6L)
pp; 6 DwgNo 1/1
Title Terms: FLASH; MEMORY; CIRCUIT; JUDGEMENT; INSPECT; DATA; DATA; READ; SIMULTANEOUS; ERROR; READ; DATA; BASED; ERROR; CORRECT; CIRCUIT; CONTROL
Derwent Class: T01; U14
International Patent Class (Main): G06F-012/16
International Patent Class (Additional): G06F-011/10; G06F-012/04; G11C-029/00
File Segment: EPI

25/5/10 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013960575 **Image available**
WPI Acc No: 2001-444789/200148
XRPX Acc No: N01-328780
Memory device for integrated circuit card, has error judging circuit to judge error in data read out from memory array, based on which error correction circuit corrects error in read out data
Patent Assignee: HITACHI LTD (HITA); KATAYAMA K (KATA-I); NAKAMURA K (NAKA-I); NOZOE A (NOZO-I)
Inventor: KATAYAMA K; NAKAMURA K; NOZOE A
Number of Countries: 004 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000305861	A	20001102	JP 99118567	A	19990426	200148	B
KR 2001029659	A	20010406	KR 200021838	A	20000425	200162	
US 6351412	B1	20020226	US 2000558036	A	20000426	200220	
			US 2000636736	A	20000811		
US 6359806	B1	20020319	US 2000558036	A	20000426	200224	
US 20020054508	A1	20020509	US 2000558036	A	20000426	200235	
			US 2000636736	A	20000811		
			US 200112525	A	20011212		
TW 479169	A	20020311	TW 2000106718	A	20000411	200309	
US 6549460	B2	20030415	US 2000558036	A	20000426	200329	
			US 2000636736	A	20000811		
			US 200112525	A	20011212		

Priority Applications (No Type Date): JP 99118567 A 19990426
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
JP 2000305861 A 11 G06F-012/16
KR 2001029659 A G06F-011/00
US 6351412 B1 G11C-016/06 Cont of application US 2000558036

US 6359806	B1	G11C-016/06		
US 20020054508	A1	G11C-016/06	Cont of application US 2000558036	
			Cont of application US 2000636736	
TW 479169	A	G06F-012/16		
US 6549460	B2	G11C-016/06	Cont of application US 2000558036	
			Cont of application US 2000636736	

Abstract (Basic): JP 2000305861 A

NOVELTY - A data register holds stored data of several memory **elements** read out from memory array (20). Error judging circuit (12) judges the presence of error in the read-out data and when there is error, read-out data is sent to error correction circuit (10) for correcting the error.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for memory card.

USE - For integrated circuit (IC) card.

ADVANTAGE - Read-out duration of data from non-volatile storage having error correction function is shortened.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of **error correction** symbol generation in **flash** memory and **error correction** circuit.

Error correction circuit (10)

Error judging circuit (12)

Memory array (20)

pp; 11 DwgNo 1/8

Title Terms: MEMORY; DEVICE; INTEGRATE; CIRCUIT; CARD; ERROR; JUDGEMENT; CIRCUIT; JUDGEMENT; ERROR; DATA; READ; MEMORY; ARRAY; BASED; ERROR; CORRECT; CIRCUIT; CORRECT; ERROR; READ; DATA

Derwent Class: T01; T04; U14

International Patent Class (Main): G06F-011/00; G06F-012/16; G11C-016/06

International Patent Class (Additional): G06F-011/10; G06K-019/07

File Segment: EPI

25/5/11 (Item 10 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012773250 **Image available**

WPI Acc No: 1999-579477/199949

XRPX Acc No: N99-427780

On- chip system for fault detection and testing of memory array e.g. DRAM

Patent Assignee: HEURISTIC PHYSICS LAB INC (HEUR-N); LSI LOGIC CORP (LSIL-N)

Inventor: IRRINKI V S; LEPEJIAN Y D

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5956350	A	19990921	US 97958775	A	19971027	199949	B

Priority Applications (No Type Date): US 97958775 A 19971027

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5956350	A		9	G06F-011/00	

Abstract (Basic): US 5956350 A

NOVELTY - A built-in self test (BIST) **module** (110) provided which applies test pattern to memory array (101) after the array is heated by heating **element** . A built-in self repair (BISR) **module** (112) intercepts access to detected faulty memory location and reroutes access to a redundant memory.

DETAILED DESCRIPTION - The heating **element** is coupled to the substrate comprising the memory array to heat the memory array to a predetermined temperature. A heating controller (120) receives temperature signal indicating memory array temperature from a temperature sensor (118) based on which power supply to the heating

element is controlled. An INDEPENDENT CLAIM is also included for method for on-chip testing and repairing of memories.

USE - For memory array e.g. DRAM.

ADVANTAGE - Performs reliable detection and repair of faulty memory locations that would not normally test faulty under initial power ON conditions, by testing the memory locations after heating the memory array to a predefined temperature.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the memory storage device.

Memory array (101)

Built-in self test **module** (110)

Built-in self repair **module** (112)

Temperature sensor (118)

Heating controller (120)

pp; 9 DwgNo 1/5

Title Terms: CHIP; SYSTEM; FAULT; DETECT; TEST; MEMORY; ARRAY; DRAM

Derwent Class: T01; U13

International Patent Class (Main): G06F-011/00

File Segment: EPI

25/5/12 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012701479 **Image available**

WPI Acc No: 1999-507588/199942

XRPX Acc No: N99-378159

FPGA controller for fault tolerant multiprocessor used in computer system

Patent Assignee: US SEC OF AIR FORCE (USAF)

Inventor: KWIAT K A

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5931959	A	19990803	US 97861252	A	19970521	199942	B

Priority Applications (No Type Date): US 97861252 A 19970521

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5931959	A		20	G06F-011/00	

Abstract (Basic): US 5931959 A

NOVELTY - The memory interface (3) is connected to the dual port memories (2), that are connected to the respective computing **modules** (1). The selected number of cells of the FPGA (4) are reprogrammed based on data stored in the ROM (6) to enable specific computing **modules** to be operated in fault tolerant mode.

DETAILED DESCRIPTION - The FPGA is connected to the interface. A controller (5) connects the FPGA to the ROM (6). INDEPENDENT CLAIMS are also included for the following:

(a) fault tolerant multiprocessing method;

(b) FPGA partial reconfiguration regulating method

USE - For fault tolerant multiprocessor used in computer system. For fault tolerance in hardware by FPGA.

ADVANTAGE - Reduces wastage of redundant resources by maximizing processor utilization. Enables selection of application like fixed priority, FIFO, round-robin algorithm in FPGA. Reduces time required to switch operation of FPGA by changing partial reconfiguration of cells. Facilitates error checking for both executive processor and coprocessor by separating fault detectors. Increases variety of fault tolerance algorithms whose complexity exceeds that of majority voting. Reduces failure rate, even if ROM is used. Enables maintenance of virtual **IC** support for **fault tolerance** and multiprocessing by FPGA without reducing reliability of system. Enables utilization of FPGA as computing **module** .

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of fault tolerance multiprocessor.

Computing **module** (1)
Dual port memory (2)
Memory interface (3)
FPGA (4)
Controller (5)
ROM (6)
pp; 20 DwgNo 1/12
Title Terms: CONTROL; FAULT; TOLERATE; MULTIPROCESSOR; COMPUTER; SYSTEM
Derwent Class: T01; U21
International Patent Class (Main): G06F-011/00
International Patent Class (Additional): G06F-011/08; **H03M-013/00**
File Segment: EPI

25/5/13 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012652229 **Image available**
WPI Acc No: 1999-458334/199938
XRPX Acc No: N99-342839

Digital signal processing used to determine positioning information from analog synchro input signals

Patent Assignee: ADVANCED DISPLAYS CORP (ADDI-N); UNIVERSAL INSTR CORP (UVIN-N); L-3 COMMUNICATIONS CORP (LTHR-N); UNIVERSAL AVIONICS SYSTEMS CORP (UVAV-N); INSTR DIV & L-3 COMMUNICATIONS (INST-N)
Inventor: ASHCRAFT K D; GOODE J W; SMITH J R
Number of Countries: 082 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9935604	A2	19990715	WO 99US469	A	19990108	199938	B
AU 9925582	A	19990726	AU 9925582	A	19990108	199952	
US 6075472	A	20000613	US 9872377	P	19980109	200035	
			US 99227456	A	19990108		
EP 1046124	A2	20001025	EP 99905425	A	19990108	200055	
			WO 99US469	A	19990108		
US 6222469	B1	20010424	US 9872377	P	19980109	200125	
			US 99227456	A	19990108		
			US 2000577024	A	20000523		

Priority Applications (No Type Date): US 9872377 P 19980109; US 99227456 A 19990108; US 2000577024 A 20000523
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9935604	A2	E	42	G06K-000/00	
Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW					
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW					
AU 9925582	A				Based on patent WO 9935604
US 6075472	A			H03M-001/48	Provisional application US 9872377
EP 1046124	A2	E		G06K-001/00	Based on patent WO 9935604
Designated States (Regional): DE FR GB IT SE					
US 6222469	B1			H03M-001/48	Provisional application US 9872377 Cont of application US 99227456 Cont of patent US 6075472

Abstract (Basic): WO 9935604 A2

NOVELTY - Analog reference (R1,R2) is applied to a position sensor (synchro) to generate analog synchro signals (S1,S2,S3) which are converted using analog-to-digital converters to provide digital inputs (X,Y,Z,REF) to the digital signal processing (DSP) **module** . The DSP **module** uses the various inputs to determine an output which will indicate, for instance, angular position or velocity.

USE - For use in determining and controlling the position, speed or

torque of rotating shafts, typically may be used in avionics instrumentation display units to determine attitude or pitch of an aircraft.

ADVANTAGE - Using a DSP **module** to generate the required status improves the accuracy and may also reduce cost by eliminating the need for special synchro-to-digital converter **chips** or other **error correcting** hardware. A generic DSP card may be used, which can easily be adapted using a field reprogrammable flash EPROM, to satisfy various customers and their changing requirements.

pp; 42 DwgNo 1,2/20

Title Terms: DIGITAL; SIGNAL; PROCESS; DETERMINE; POSITION; INFORMATION; ANALOGUE; SYNCHRONOUS; INPUT; SIGNAL

Derwent Class: T01; T06; W06

International Patent Class (Main): G06K-000/00; G06K-001/00; **H03M-001/48**

File Segment: EPI

25/5/14 (Item 13 from file: 350)

012611939 **Image available**

WPI Acc No: 1999-418043/199935

Related WPI Acc No: 2001-606652; 2002-488969

XRPX Acc No: N99-312034

Error correction **unit for** DRAM module **in data processing system**

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)

Inventor: SEYYEDY M

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5923682	A	19990713	US 97790463	A	19970129	199935	B

Priority Applications (No Type Date): US 97790463 A 19970129

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5923682	A		8	G11C-029/00	

Abstract (Basic): US 5923682 A

NOVELTY - An error correction circuitry (300) is located between DRAM units (100) and the communication path. The DRAM units are sorted such that there is zero correlation of failing memory cells among the memory devices in a single memory **module** before they are included in the memory **module** .

DETAILED DESCRIPTION - A communication path is provided for bidirectional data communication between independently addressable DRAM units (100) and an external circuit. The error correction circuitry operates according to error correction process.

INDEPENDENT CLAIMS are also included for the following:

(a) a populating method of a memory **module** ;

(b) an error free communication method with the memory **module** .

USE - In data processing system.

ADVANTAGE - The error correction circuitry identifies and corrects errors in communication between memory **module** and external processor, thus reliable data processing system is offered.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of single inline memory **module** incorporating the error correction unit.

DRAM units (100)

Error correction circuitry (300)

pp; 8 DwgNo 3/5

Title Terms: ERROR; CORRECT; UNIT; DRAM; **MODULE** ; DATA; PROCESS; SYSTEM

Derwent Class: U11; U14

International Patent Class (Main): G11C-029/00

File Segment: EPI

25/5/15 (Item 14 from file: 350)

DIALOG(R)File 350:Derwent WPIX
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012608803 **Image available**
WPI Acc No: 1999-414907/199935
XRPX Acc No: N99-310995
Data error corrector for CD- ROM decoder - includes error correction circuit, which corrects syndrome of vector number on specific series
Patent Assignee: TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11168392	A	19990622	JP 97334539	A	19971204	199935	B

Priority Applications (No Type Date): JP 97334539 A 19971204
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11168392	A		18	H03M-013/00	

Abstract (Basic): JP 11168392 A
NOVELTY - A calculator (4) calculates the syndrome of Q and P series of data sector and stores it in memory (5). The mistake for error position on the series is detected, based on the stored data and data corrector value is calculated. Vector number and error position of another series is generated and the error correction circuit (6) corrects the syndrome of the vector number on another series. DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for data error correction method.
USE - For CD-ROM decoder.
ADVANTAGE - High speed error correction is done by small bandwidth memory device, since wasteful repeating correction is not done.
DESCRIPTION OF DRAWING(S) - The figure shows the entire **component** of data error correction apparatus. (4) Calculation circuit; (5) Memory; (6) Error correction circuit.
Dwg.1/12
Title Terms: DATA; ERROR; CORRECT; CD; ROM; DECODE; ERROR; CORRECT; CIRCUIT ; CORRECT; SYNDROME; VECTOR; NUMBER; SPECIFIC; SERIES
Derwent Class: T03; U21
International Patent Class (Main): **H03M-013/00**
International Patent Class (Additional): G11B-020/18
File Segment: EPI

25/5/16 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011910400 **Image available**
WPI Acc No: 1998-327310/199829
XRPX Acc No: N98-256121
Printer with non-volatile EEPROM for error correction - corrects error generated during printing using error correction data stored in EEPROM
Patent Assignee: HITACHI KOKI KK (HITO)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10119367	A	19980512	JP 96283728	A	19961025	199829	B

Priority Applications (No Type Date): JP 96283728 A 19961025
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10119367	A		3	B41J-005/30	

Abstract (Basic): JP 10119367 A
The printer includes a printing mechanism (1) which is controlled by a controller (3). An EEPROM (6) is provided in which data for error

correction is stored. The error generated during printing is corrected by using the error correction data.

ADVANTAGE - Protects various set value at time of sum check error generation of EEPROM without cost and **component** increase.

Dwg.1/4

Title Terms: PRINT; NON; VOLATILE; EEPROM; ERROR; CORRECT; CORRECT; ERROR; GENERATE; PRINT; ERROR; CORRECT; DATA; STORAGE; EEPROM

Derwent Class: P75; T01; T04

International Patent Class (Main): B41J-005/30

International Patent Class (Additional): G06F-003/12

File Segment: EPI; EngPI

25/5/17 (Item 16 from file: 350)

DIALOG(R)File 350:Derwent WPIX

010481331 **Image available**

WPI Acc No: 1995-382652/199549

XRPX Acc No: N95-280305

Error location determining circuit for optical disc memory - multiplies each component **signal by respective** element **of set of Galois file** elements

Patent Assignee: MITSUBISHI SEMICONDUCTOR AMERICA INC (MITS-N)

Inventor: GIBBS V L; KAO R

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5463642	A	19951031	US 9382867	A	19930629	199549	B

Priority Applications (No Type Date): US 9382867 A 19930629

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5463642	A		25	H03M-013/00	

Abstract (Basic): US 5463642 A

The circuit tests each possible error location using an error location polynomial. Accumulating registers of a set of multiplier accumulators are loaded with the **components** of the error location polynomial at the start of each 120-byte word to be tested. The output signals of the accumulating registers are transferred to an XOR check-sum circuit.

If the output of the XOR checksum circuit is determined to be zero, the current byte of the tested word is considered to be an error location. An external clock signal corresponding to the consecutive bytes to be tested saves the outputs of the unary multipliers for multiplying by the Galois field **elements** alpha123-alpha131, through a feedback loop to the multiplier accumulating registers.

ADVANTAGE - Reduced testing time. REduces area of **error correction chip** .

Dwg.3/20

Title Terms: ERROR; LOCATE; DETERMINE; CIRCUIT; OPTICAL; DISC; MEMORY; MULTIPLICATION; **COMPONENT** ; SIGNAL; RESPECTIVE; **ELEMENT** ; SET; GALOIS; FILE; **ELEMENT**

Derwent Class: T01; T03; U21

International Patent Class (Main): **H03M-013/00**

File Segment: EPI

25/5/18 (Item 17 from file: 350)

DIALOG(R)File 350:Derwent WPIX

004667707

WPI Acc No: 1986-171049/198627

XRPX Acc No: N86-127696

Integrated circuit error - correcting **circuit - uses syndrome word**

with K-I bits to correct up to one error in M-bit data field having associated K parity bits

Patent Assignee: SGS THOMSON MICROELTRN INC (SGSA); THOMSON COMP MOSTEK (MOSS); THOMSON COMPONENTS-MOSTEK CORP (MOSS)

Inventor: PROEBSTING R J

Number of Countries: 004 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 186588	A	19860702	EP 85402566	A	19851220	198627	B
JP 61221834	A	19861002	JP 85299604	A	19851226	198646	
US 4649540	A	19870310	US 84686333	A	19841226	198712	
EP 186588	B1	19930317	EP 85402566	A	19851220	199311	
DE 3587190	G	19930422	DE 3587190	A	19851220	199317	
			EP 85402566	A	19851220		
KR 9503518	B1	19950413	KR 859817	A	19851226	199709	

Priority Applications (No Type Date): US 84686333 A 19841226

Cited Patents: A3...8910; No-SR.Pub; US 3534331; US 3825893; US 4345328

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 186588	A	E	24		
EP 186588	B1	E	13	H03M-013/00	
DE 3587190	G			H03M-013/00	Based on patent EP 186588
KR 9503518	B1			H04L-001/00	

Abstract (Basic): EP 186588 B

The circuit corrects up to one error in a data field carried by M data signals on a set of data lines in a region of an integrated circuit. Each set of data lines has a sequential binary data address representative of the location of that data line within the set of data lines. The circuit includes a set of parity lines carrying a set of K parity signals formed in a given manner from a set of input data signals. K is the least integar that satisfies the relationship :2 Power k is greater than or equal to M+k+1. Parity circuitry combines the set of parity signals and the data signals in a given manner to generate a binary syndrome word having K-1 bits.

A single data signal located at a binary error address specified by the contents of the syndrome word is then corrected.

ADVANTAGE - Provides simplified decoding scheme to correct single error in data field by simplifying routing problem. Allows memory, in principle, to have one defect in every row of chip and still have a working chip. (24pp Dwg.No.4/4)

Title Terms: INTEGRATE; CIRCUIT; ERROR; CORRECT; CIRCUIT; SYNDROME; WORD; BIT; CORRECT; UP; ONE; ERROR; BIT; DATA; FIELD; ASSOCIATE; PARITY; BIT

Derwent Class: U13; U14; U21

International Patent Class (Main): **H03M-013/00** ; H04L-001/00

International Patent Class (Additional): G06F-011/10

File Segment: EPI

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Set     Items   Description
S1    2582964   MODULE? ? OR COMPONENT? ? OR ELEMENT? ? OR ROUTINE? ?
S2      82155   (FIRST OR 1ST OR PRIME OR PRIMARY OR INITIAL OR LEAD??? OR
             MAIN OR DOMINANT OR CARDINAL OR ORIGINAL)(2N)S1
S3      13513   (SECOND OR 2ND)(2N)S1
S4      14166   (THIRD OR 3RD)(2N)S1
S5       2639   (FOURTH OR 4TH)(2N)S1
S6      92397   ERROR()(CORRECT??? OR CONTROL) OR ECC OR FAULT()(TOLERAN? -
             OR DETECTION)
S7    4896504   CHIP? ? OR MICROCHIP OR INTEGRATED()CIRCUIT? OR IC OR RAM -
             OR RANDOM()ACCESS()MEMORY OR DRAM? OR SRAM? OR ROM? OR PROM? -
             OR EPROM? OR EEPROM? OR FLASH
S8   14284185   COUPLE? OR CONNECT? OR LINK? OR JOIN? OR UNITE?
S9     261198   STUB OR STUBS OR ROUTINE?
S10      2888   S6 (3N) S7
S11       352   S1 (S) S10
S12         0   S2 (S) S3 (S) S4 (S) S5 (S) S10
S13        12   S2 (S) S10
S14         0   S3 (S) S10
S15         0   S4 (S) S10
S16         0   S5 (S) S10
S17         1   S11 (S) S8 (S) S9
S18        13   S13 OR S17
S19        12   S18 NOT PY>2001
S20        12   S19 NOT PD>20010723
S21         9   RD (unique items)
File  15:ABI/Inform(R) 1971-2004/Mar 27
         (c) 2004 ProQuest Info&Learning
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 647:CMP  Computer Fulltext 1988-2004/Mar W3
         (c) 2004 CMP Media, LLC
File 275:Gale Group Computer DB(TM) 1983-2004/Mar 30
         (c) 2004 The Gale Group
File 674:Computer News Fulltext 1989-2004/Mar W3
         (c) 2004 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2004/Mar 30
         (c) 2004 The Dialog Corp.
File 624:McGraw-Hill Publications 1985-2004/Mar 29
         (c) 2004 McGraw-Hill Co. Inc
File 636:Gale Group Newsletter DB(TM) 1987-2004/Mar 30
         (c) 2004 The Gale Group
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 613:PR Newswire 1999-2004/Mar 30
         (c) 2004 PR Newswire Association Inc
File  16:Gale Group PROMT(R) 1990-2004/Mar 30
         (c) 2004 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 553:Wilson Bus. Abs. FullText 1982-2004/Feb
         (c) 2004 The HW Wilson Co
```

21/5,K/1 (Item 1 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

01489374 01-40362
USE FORMAT 9 FOR FULL TEXT

CD-ROM drive manufacturing

Traub, Rie

EMedia Professional v10n9 PP: 54-63+ Sep 1997 ISSN: 1090-946X
JRNL CODE: LDP
DOC TYPE: Journal article LANGUAGE: English LENGTH: 13 Pages
SPECIAL FEATURE: Charts Graphs
WORD COUNT: 4463

ABSTRACT: Today, with CD-ROM drives integrated into almost every desktop computer model, new notebook computers, a growing roster of jukeboxes and towers, disc-based game machines, and CD/online hybrid set-top boxes, dramatically increased demand has attracted a host of players to the drive-manufacturing game. Today CD-ROM is hardly the only game in town, and manufactures are adding DVD-ROM, DVD-R, DVD-RW, and DVD-RAM to their family of CD-based hardware products. It is predicted that in just 2 years, the installed base of CD-ROM and DVD-ROM will be 202 million units. Despite the consumer perception about branded CD-ROM drives, drive manufacturers tend to specialize in producing one or only a few parts of a CD-ROM drive's components, making mechanisms or chipsets that are sold to OEMs in quantity, and priced according to what the market will bear. Most CD-ROM drive manufacturers and industry analysts see price as the major deciding factor in the change-over to DVD-ROM from CD-ROM in the next several years.

DESCRIPTORS: CD-ROM; Digital videodisk; Disk drives; Industrywide conditions; Manycompanies; Trends
CLASSIFICATION CODES: 8650 (CN=Electrical & electronics industries); 5230 (CN=Computer hardware)

...TEXT: notebooks. Manabu Sata of Sanyo's OEM Marketing Department says Sanyo develops and produces many of the **main components** of CD-ROM drives, such as the optical pick-up mechanisms, the semiconductor elements (including the servo **IC** and **error - correction IC**), and the spindle motors. But the remaining drive components, like interface cards and box casings, are outsourced...

21/5,K/2 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01140857 CMP ACCESSION NUMBER: NWC19971001S0031

Don't Blink! You Might Miss The First Gigabit Products

Joel Conover

NETWORK COMPUTING, 1997, n 818, PG122
PUBLICATION DATE: 971001
JOURNAL CODE: NWC LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Reviews
WORD COUNT: 3567

TEXT:

When "Fast" just isn't fast enough, it's time to think Gigabit. Network Computing recently had the opportunity to test five vendors' Gigabit Ethernet products in our University of Wisconsin lab. These are the first of their kind-literally; some of the units we tested were early production models and first customer shipments. What did we find? If you are considering this bleeding-edge technology for your network, look out. Not all products are created equal; performance and interoperability are key in this early market.

COMPANY NAMES (DIALOG GENERATED): AceNIC ; Alteon Networks ; Bay Networks ; Cabletron Systems ; Cisco Systems ; Digital Equipment Corp ; Essential

Communications ; Extreme Networks ; Flow Control ; Foundry Networks ; Ganymede Software ; Gigabit Ethernet ; GigaLabs ; Hewlett Packard Co ; Internet Group Management ; IBM Corp ; Media Access Control ; Netcom Systems ; Network Computing Online ; NBase Communications ; Packet Engines ; Plaintree Systems ; Prominet Corp ; PCI ; Silicon Graphics ; Sun Microsystems ; University of Wisconsin ; XLNT ; 3Com Corp

... a 10-port 100BASE-FX module and a 20-port 10/100 twisted-pair blade. The Supervisor **module** occupies the **first** slot of the chassis, and the remaining six slots can be populated with up to 120 10...

...24 Gigabit Ethernet ports. An optional redundant Supervisor module can be placed in the second slot for **fault tolerance** . The **Prominet** switch offers significant performance advantages over the XLNT product in the gigabit switch market. Specifically, the Prominet...

21/5,K/3 (Item 2 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01059852 CMP ACCESSION NUMBER: EET1995072450031
Northwest startup blazes custom-silicon trail (News Briefs)
Ron Wilson
ELECTRONIC ENGINEERING TIMES, 1995, n 858, PG27
PUBLICATION DATE: 950724
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: news/Business
WORD COUNT: 895.
TEXT:
Pullman, Wash. - The Palouse is high, rolling country. The wind drives unimpeded across wheat fields. Two-lane roads wind among the hills, occasionally descending into tiny towns with fanatically enforced speed limits.

... way to get in the door, not a complete product. Most of AHA's designs are multifunction **chips** , of which its **error - correction** code or compression hardware is a progressively smaller **component** .
"At **first** , just doing the ECC was the hard job," Owsley said. "But now, if you look at our...

21/5,K/4 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02272103 SUPPLIER NUMBER: 53948498 (USE FORMAT 7 OR 9 FOR FULL TEXT)
PC Briefs 02/23/99.
Newsbytes, NA
Feb 23, 1999
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 746 LINE COUNT: 00062

COMPANY NAMES: Intel Corp.
GEOGRAPHIC CODES/NAMES: 1U9CA California
EVENT CODES/NAMES: 336 Product introduction
PRODUCT/INDUSTRY NAMES: 3674000 (Semiconductor Devices); 3573000 (Computers & Peripherals)
SIC CODES: 3674 Semiconductors and related devices; 3571 Electronic computers
NAICS CODES: 334413 Semiconductor and Related Device Manufacturing; 334111 Electronic Computer Manufacturing
TICKER SYMBOLS: INTC
FILE SEGMENT: NW File 649

TEXT:

...GB) per second using 800 megahertz (MHz) RIMM. Kingston says it has shipped more than 7,000 **modules** to **leading** **original** equipment manufacturers (OEMs) so far and can easily ramp up production to match Intel's 1999 PC...

...S.A. Hyundai Electronics says its 64 megabit (Mb) Rambus dynamic RAM (DRAM) and new 64 Mb **ECC** Rambus **DRAM** (RDRAM) products will be available next quarter. The new products, the HYRD64E840 and HYRD72E840 series, are 0

21/5,K/5 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01900197 SUPPLIER NUMBER: 17982199 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Pricey performer. (AT and T's S40 server)(Networks for the '90s) (Hardware Review)(Evaluation)(Brief Article)
Kennedy, Randall C.; Meyerson, Adam
PC/Computing, v9, n3, p164(1)
March, 1996
DOCUMENT TYPE: Evaluation Brief Article ISSN: 0899-1847
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 381 LINE COUNT: 00034

SPECIAL FEATURES: illustration; photograph; table
COMPANY NAMES: AT and T Global Information Solutions--Products
DESCRIPTORS: Hardware Single Product Review; Pentium-Based System
SIC CODES: 3571 Electronic computers
TRADE NAMES: AT and T Globalyst S40 (Pentium-based system)--Evaluation
FILE SEGMENT: CD File 275

... as the number of active clients increased from 12 to 60.
The system's documentation and its **components** are all **first** -rate. They include Mylex's PCI-based DAC960 SCSI-2 RAID controller with 4MB of dedicated cache...
...in hot-swappable drive bays. Like the servers from HP and Compaq, AT&T's S40 features **ECC** **RAM** . In addition, the S40 includes 1MB of dedicated L2 cache for each processor, which kept its performance...

21/5,K/6 (Item 1 from file: 674)
DIALOG(R)File 674:Computer News Fulltext

076171
Livermore: Response to firewall RFP
Journal: Network World
Publication Date: July 19,. 1999
Word Count: 1396 Line Count: 139

Text:
... over function (fwpulse) is able to avoid unnecessary takeovers caused by transient network conditions. When the fwpulse **routine** determines a take over is required the process occurs within the blink of an eye. The take...

...can be customized with pre- and post- takeover scripts. Each computer is manufactured using the highest quality **components** available. For example, the motherboards on the PORTUS-ES(m) have demonstrated Mean Time Between Failures of...

... fly. Product architecture isolates errors and prevents them from propagating from function to function. Specialized function recovery **routines** dynamically restart a function should it fail. Automatic function retirement returns all resources acquired from the system...
... a periodic basis. This prevents system disruptions caused by resource

depletion such as memory leaks. Functional recovery **routines** dynamically restart the retired function to avoid any service disruptions. Hardware and software errors are logged. Certain...

...workload. The PORTUS-ES22i systems proposed for each remote location are also capable of saturating a T3 **link** . The software is capable of supporting more than 60,000 concurrent user sessions. The ultimate constraint is...

... has an API that allows customization to enhance special applications. The API allows customized code to control **connection** authorization. The API allows access to data in the buffer from the client and server. This allows...

... single system.LoggingPORTUS performs extensive logging of all access attempts. A log record is written for each **connection** and after each disconnect. The log information includes date, time, client hostname and IP address, server hostname and IP address, The duration of the **connection** the number of bytes sent and received and even the CPU time used for longer running **connections** . CPU time is not recorded for HTTP access as the average time used per **connection** is less than the CPU timer resolution. Applications that require user identification and authentication such as telnet... systems each with the following configuration.Single 400 MHz PowerPlus 604e processor, 512kB L2 cache,512 MB **ECC** **RAM** , Ultra 2 SCSI adapter,hot swap 9 GB Ultra2 SCSI disksdual hot swap 300 watt power supplies...

...two systems each with the following configuration.Single 400 MHz Pentium II, 512kB L2 cache,512 MB **ECC** **RAM**, Ultra 2 SCSI adapter,hot swap 9 GB Ultra2 SCSI disksdual hot swap 300 watt power supplies...

21/5,K/7 (Item 1 from file: 16)

05396446 Supplier Number: 50358018 (USE FORMAT 7 FOR FULLTEXT)
Bad things happen to good power
Ruff, Harold
European Power News, p20
Nov, 1997
ISSN: 0261-8214
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Tabloid; Trade
Word Count: 4087
PUBLISHER NAME: FMJ International Publications Ltd.
EVENT NAMES: *330 (Product information)
GEOGRAPHIC NAMES: *4EUUK (United Kingdom)
PRODUCT NAMES: **3629201 (Uninterruptible Power Supplies)
INDUSTRY NAMES: BUSN (Any type of business); INTL (Business, International); OIL (Petroleum, Energy Resources and Mining)
NAICS CODES: 335999 (All Other Miscellaneous Electrical Equipment and Component Manufacturing)

... UPS vendor must avoid several potential problems which could render the system less reliable than the others.

First , the UPS **module** must have flexible, reliable controls. The Liebert Series 600 UPS has a clear advantage here. Liebert designers...

...ASICs). These ASICs replace the failure prone discrete logic boards used by all competing units. The ASIC **chips** have redundant (single **fault tolerant**) internal architecture, and are used both in the UPS modules and system control cabinets.

Second, the two...

21/5,K/8 (Item 2 from file: 16)

DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2004 The Gale Group. All rts. reserv.

05266178 Supplier Number: 48024140 (USE FORMAT 7 FOR FULLTEXT)
Don't Blink! You Might Miss The First Gigabit Products
Conover, Joel
Network Computing, p122
Oct 1, 1997
ISSN: 1046-4468
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 3599
PUBLISHER NAME: CMP Publications, Inc.
COMPANY NAMES: *Alteon Networks Inc.; Essential Communications Corp.; Foundry Networks Inc.; Prominet Corp.
EVENT NAMES: *350 (Product standards, safety, & recalls)
GEOGRAPHIC NAMES: *1USA (United States)
PRODUCT NAMES: *3661250 (Data Communications Systems)
INDUSTRY NAMES: BUSN (Any type of business); CMPT (Computers and Office Automation)
NAICS CODES: 33421 (Telephone Apparatus Manufacturing)
SPECIAL FEATURES: COMPANY

... a 10-port 100BASE-FX module and a 20-port 10/100 twisted-pair blade. The Supervisor **module** occupies the **first** slot of the chassis, and the remaining six slots can be populated with up to 120 10...

...24 Gigabit Ethernet ports. An optional redundant Supervisor module can be placed in the second slot for **fault tolerance** . The **Prominet** switch offers significant performance advantages over the XLNT product in the gigabit switch market. Specifically, the Prominet...

21/5,K/9 (Item 3 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2004 The Gale Group. All rts. reserv.

03931937 Supplier Number: 45684728 (USE FORMAT 7 FOR FULLTEXT)
Northwest startup blazes custom-silicon trail
Electronic Engineering Times, p27
July 24, 1995
ISSN: 0192-1541
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 900
PUBLISHER NAME: CMP Publications, Inc.
COMPANY NAMES: *Advanced Hardware Architectures Inc.
EVENT NAMES: *220 (Strategy & planning)
GEOGRAPHIC NAMES: *1U9WA (Washington)
PRODUCT NAMES: *3674180 (Integrated Circuits by Function)
INDUSTRY NAMES: BUSN (Any type of business); ELEC (Electronics); ENG (Engineering and Manufacturing)
NAICS CODES: 334413 (Semiconductor and Related Device Manufacturing)
SPECIAL FEATURES: COMPANY

... way to get in the door, not a complete product. Most of AHA's designs are multifunction **chips** , of which its **error** - **correction** code or compression hardware is a progressively smaller **component** .
"At **first** , just doing the ECC was the hard job," Owsley said. "But now, if you look at our...

```
Set     Items   Description
S1        140   AU='MCCALL J' OR AU='MCCALL J A' OR AU='MCCALL J A JR' OR -
            AU='MCCALL JAMES A'
S2        122   AU='MCCALL, J' OR AU='MCCALL, J.' OR AU='MCCALL, J. A.' OR
            AU='MCCALL, J. A. W.' OR AU='MCCALL, J.A.' OR AU='MCCALL, J.A-
            .W.' OR AU='MCCALL, JAMES' OR AU='MCCALL, JAMES A.'
S3         12   AU='LEDDIGE M' OR AU='LEDDIGE, M' OR AU='LEDDIGE, M.' OR A-
            U='LEDDIGE, MIKE'
S4          2   AU='LEDDIGE M'
S5        270   S1 OR S2 OR S3 OR S4
S6          1   S5 AND MODULE?
S7          0   S5 AND SHARING()TERMINATION?
S8          2   S5 AND ERROR CORRECTION
S9          1   (S1 OR S2) AND (S3 OR S4)
S10         4   S6 OR S8 OR S9
File   2:INSPEC 1969-2004/Mar W3
         (c) 2004 Institution of Electrical Engineers
File   6:NTIS 1964-2004/Mar W4
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
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         (c) 2004 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2004/Feb
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/Mar W4
         (c) 2004 BLDSC all rts. reserv.
File  92:IHS Intl.Stds.& Specs. 1999/Nov
         (c) 1999 Information Handling Services
File  94:JICST-EPlus 1985-2004/Mar W2
         (c)2004 Japan Science and Tech Corp(JST)
File  95:TEME-Technology & Management 1989-2004/Mar W1
         (c) 2004 FIZ TECHNIK
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Feb
         (c) 2004 The HW Wilson Co.
File 103:Energy SciTec 1974-2004/Mar B1
         (c) 2004 Contains copyrighted material
File 144:Pascal 1973-2004/Mar W3
         (c) 2004 INIST/CNRS
File 202:Info. Sci. & Tech. Abs. 1966-2004/Feb 27
         (c) 2004 EBSCO Publishing
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File 239:Mathsci 1940-2004/Apr
         (c) 2004 American Mathematical Society
File 275:Gale Group Computer DB(TM) 1983-2004/Mar 30
         (c) 2004 The Gale Group
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File 647:CMP  Computer Fulltext 1988-2004/Mar W3
         (c) 2004 CMP Media, LLC
File 674:Computer News Fulltext 1989-2004/Mar W3
         (c) 2004 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2004/Mar 30
         (c) 2004 The Dialog Corp.
```

10/5,K/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7434023 INSPEC Abstract Number: B2002-12-2550G-037, C2002-12-7410D-071
Title: Integrated method of mask data checking and inspection data prep for manufacturable mask inspection: inspection rule violations
Author(s): **McCall, J.** ; Reddy, V.; Hyung Min Kim; Babasa, M.
Author Affiliation: Intel Corp., Santa Clara, CA, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.4562 p.161-70
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 2002 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(2002)4562L.161:IMMD;1-U
Material Identity Number: C574-2002-170
U.S. Copyright Clearance Center Code: 0277-786X/02/$15.00
Conference Title: 21st Annual BACUS Symposium on Photomask Technology
Conference Sponsor: SPIE
Conference Date: 3-5 Oct. 2001 Conference Location: Monterey, CA, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Practical (P); Experimental (X)
Abstract: Many mask patterns contain small un-inspectable features (inspection rule violations or IRVs) that create significant through-put time (TPT) impact at mask inspection due to excessive false defects. These small features include a) drawn test designs purposely intended to be small for evaluating process capabilities, and b) un-intended small features that result from errors such as overlap of designs, gaps between cells or synthesis errors. Typically, an IRV is a feature smaller than the minimum feature size capability of the mask inspection tool. This paper describes an integrated method to find such IRVs in the data and either fix them or declare that area as not inspectable. The method includes documented drawn size limits for inspectability, data checks at drawn level, data checks at post-fracture, and functions to define "do not inspect regions (DNIRs)" for any remaining IRVs in the data. Data checking at post-fracture must comprehend optical proximity correction (OPC), which generates small features that are not IRVs. The defined DNIRs are listed in the jobdeck for automated inspection data preparation with no engineering intervention. The result is improved mask inspection TPT as well as early detection and correction of certain design or synthesis errors. (2 Refs)
Subfile: B C
Descriptors: data preparation; fault location; inspection; integrated circuit manufacture; integrated circuit reliability; masks; photolithography; proximity effect (lithography)
Identifiers: mask data checking; inspection data preparation; manufacturable mask inspection; inspection rule violations; mask patterns; un-inspectable features; IRV; mask inspection through-put time impact; TPT; false defects; process evaluation drawn test designs; design overlap errors ; cell gaps; synthesis error detection; mask inspection tool minimum feature size capability; noninspectable areas; **error correction** ; documented inspection drawn size limits; drawn level data checks; post-fracture data checks; do not inspect regions; DNIR; optical proximity correction; OPC; jobdeck listing; automated inspection data preparation
Class Codes: B2550G (Lithography (semiconductor technology)); B2570 (Semiconductor integrated circuits); B0170E (Production facilities and engineering); B0170L (Inspection and quality control); B0170N (Reliability) ; C7410D (Electronic engineering computing)

Author(s): **McCall, J.** ; Reddy, V.; Hyung Min Kim; Babasa, M.
...Identifiers: **error correction**

10/5,K/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6856018 INSPEC Abstract Number: B2001-04-2210B-003
Title: Using routing techniques to minimize skew
Author(s): Horne, B.; **Leddige, M.**
Journal: Printed Circuit Design vol.16, no.12 p.24-7
Publisher: Miller Freeman,
Publication Date: Dec. 1999 Country of Publication: USA
CODEN: PCIDEU ISSN: 0884-9862
SICI: 0884-9862(199912)16:12L.24:URTM;1-E
Material Identity Number: I879-2001-002
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Proper routing techniques are crucial to the design of PCBs such as Direct RDRAM. By paying critical attention to design strategy, you can incorporate routing procedures that remove systematic sources of skew from your design. Some of the techniques that are especially useful in memory system design include minimizing the number and severity of bends in the lines, minimizing line discontinuities by reducing neck-down, using exact trace length matching to minimize timing skew due to routing, matching the number of vias on each line, and using ground shielding for signal trace separation. These same techniques can be applied to RIMM **modules** or other high-speed designs. (0 Refs)
Subfile: B
Descriptors: network routing; printed circuit design; random-access storage
Identifiers: routing technique; skew minimization; PCB design; Direct RDRAM; memory system; RIMM **module** ; high-speed design
Class Codes: B2210B (Printed circuit layout and design); B1265D (Memory circuits)

Author(s): Horne, B.; **Leddige, M.**
...Abstract: line, and using ground shielding for signal trace separation. These same techniques can be applied to RIMM **modules** or other high-speed designs.
...Identifiers: RIMM **module** ;

10/5,K/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6577096 INSPEC Abstract Number: B2000-06-1265D-013, C2000-06-5610S-001
Title: Physical layer design of a 1.6 GB/s DRAM bus
Author(s): Moncayo, A.; Hindi, S.; Ching-Chao Huang; Kollipara, R.; Haw-Jyh Liaw; Nguyen, D.; Perino, D.; Sarfaraz, A.; Yuan, C.; **Leddige, M.** ; **McCall, J.** ; Xang Moua; Salmon, J.
Author Affiliation: Rambus Inc., Mountain View, CA, USA
Conference Title: IEEE 8th Topical Meeting on Electrical Performance of Electronic Packaging (Cat. No.99TH8412) p.11-14
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA xii+266 pp.
ISBN: 0 7803 5597 0 Material Identity Number: XX-2000-00011
U.S. Copyright Clearance Center Code: 0 7803 5597 0/99/$10.00
Conference Title: IEEE 8th Topical Meeting on Electrical Performance of Electronic Packaging
Conference Sponsor: IEEE Microwave Theory & Tech. Soc.; IEEE Components, Packaging & Manuf. Technol. Soc
Conference Date: 25-27 Oct. 1999 Conference Location: San Diego, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Theoretical (T)
Abstract: This paper describes an innovative design and modeling methodology for development of a high performance memory bus with data signaling bandwidth of up to 1.6 gigabytes per second. Data signals operate at 800 megabits per second transfer rate. The clock frequency is 400 MHz

and the signal edge transition time is 200 ps. Due the extremely high frequencies involved, overall system electrical performance must be optimized. By following the methodology outlined in this paper, good correlation was obtained between simulated and measured results. (3 Refs)

Subfile: B C

Descriptors: clocks; digital simulation; DRAM chips; integrated circuit design; integrated circuit packaging; optimisation; system buses

Identifiers: physical layer design; DRAM bus; design/modeling methodology ; memory bus; data signaling bandwidth; data signals; transfer rate; clock frequency; signal edge transition time; system electrical performance; system electrical performance optimization; 16 Gbit/s; 800 Mbit/s; 400 MHz; 200 ps

Class Codes: B1265D (Memory circuits); B2570 (Semiconductor integrated circuits); B1265A (Digital circuit design, modelling and testing); B0170J (Product packaging); C5610S (System buses); C5320G (Semiconductor storage)

Numerical Indexing: bit rate 1.6E+10 bit/s; bit rate 8.0E+08 bit/s; frequency 4.0E+08 Hz; time 2.0E-10 s

...Author(s): S.; Ching-Chao Huang; Kollipara, R.; Haw-Jyh Liaw; Nguyen, D.; Perino, D.; Sarfaraz, A.; Yuan, C.; **Leddige, M.** ; **McCall, J.** ; Xang Moua; Salmon, J.

10/5,K/4 (Item 1 from file: 95)

01325051 I99071758300

Universal protection and control applied to a 3-breaker transfer scheme

Day, T; **McCall, J** ; Gomes, D
Cooper Power Syst., Franksville, WI, USA

1999 IEEE Transmission and Distribution Conference (Cat. No. 99CH36333), 11-16 April 1999, New Orleans, LA, USA1999
Document type: Conference paper Language: English
Record type: Abstract
ISBN: 0-7803-5515-6

ABSTRACT:
A new modular hardware and software based protection and control system has been developed to be more flexible and economical than conventional relay platforms for the development of custom protection and control schemes. The system includes a computer aided engineering (CAE) package to permits rapid customization of the scheme's logic and protective elements. An embedded virtual test system allows for rapid debugging and testing. To demonstrate the system, a 3-breaker transfer scheme was developed to replace an older, existing transfer scheme based on discrete protective and logic device. This scheme integrates the transfer logic and the protective relaying functions in to one microprocessor based device.

DESCRIPTORS: CIRCUIT BREAKERS; CAE--COMPUTER AIDED ENGINEERING; POWER SYSTEM PROTECTION; RELAY PROTECTION; **ERROR CORRECTION** ; MICROPROCESSORS; POWER SYSTEMS CONTROL
IDENTIFIERS: ENERGIENETZSTAFFELUNG; ENERGIENETZAUTOMATISIERUNG; SCHUTZRELAISEINSATZ; Leistungsschalter; Cae (Rechnerunterstuetzte Technik)

Day, T; **McCall, J** ; Gomes, D
...DESCRIPTORS: COMPUTER AIDED ENGINEERING; POWER SYSTEM PROTECTION; RELAY PROTECTION; **ERROR CORRECTION** ; MICROPROCESSORS; POWER SYSTEMS CONTROL

```
Set     Items   Description
S1         19   AU='MCCALL J' OR AU='MCCALL J A'
S2         23   AU='LEDDIGE M' OR AU='LEDDIGE M W' OR AU='LEDDIGE MICHAEL'
                  OR AU='LEDDIGE MICHAEL W'
S3         34   S1 OR S2
File 347:JAPIO Nov 1976-2003/Nov(Updated 040308)
         (c) 2004 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2004/Mar W03
         (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040325,UT=20040318
         (c) 2004 WIPO/Univentio
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200419
         (c) 2004  Thomson Derwent
```

3/5/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01069931
A VERTICAL CONNECTOR BASED PACKAGING SOLUTION FOR INTEGRATED CIRCUITS
PACKUNGSLOSUNG BASIERT AUF VERTIKALEN VERBINDUNGSLEITER FUR INTEGRIERTE SCHALTUNGEN
PROCEDE DE CONDITIONNEMENT UTILISANT DES CONNECTEURS VERTICAUX POUR CIRCUITS INTEGRES
PATENT ASSIGNEE:
INTEL CORPORATION, (322933), 2200 Mission College Boulevard, Santa Clara, CA 95052, (US), (Applicant designated States: all)
INVENTOR:
HOLMAN, Thomas, J., 3045 N.W. Baver Woods, Portland, OR 97229, (US)
LEDDIGE, Michael, W. , 15820 S.W. Galena Way, Beaverton, OR 97007, (US
LEGAL REPRESENTATIVE:
Molyneaux, Martyn William et al (34019), Harrison Goddard Foote 40-43 Chancery Lane, London WC2A 1JA, (GB)
PATENT (CC, No, Kind, Date): EP 1051748 A1 001115 (Basic)
WO 9935686 990715
APPLICATION (CC, No, Date): EP 98964295 981221; WO 98US27517 981221
PRIORITY (CC, No, Date): US 2775 980105
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: H01L-023/02; H01L-023/043; H01L-023/047; H01L-023/053; H01L-023/057; H01L-023/12; H05K-001/11; H05K-001/14; H05K-007/02; H05K-007/06; H05K-007/20
NOTE:
No A-document published by EPO
LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	001115	A1	Published application with search report
Application:	990915	A1	International application. (Art. 158(1))
Change:	040303	A1	Legal representative(s) changed 20040116
Change:	010905	A1	Legal representative(s) changed 20010718
Examination:	001115	A1	Date of request for examination: 20000712
Search Report:	020529	A1	Date of drawing up and dispatch of supplementary:search report 20020412
Change:	020529	A1	International Patent Classification changed: 20020408
Change:	020529	A1	International Patent Classification changed: 20020408
Application:	990915	A1	International application entering European phase

LANGUAGE (Publication,Procedural,Application): English; English; English

3/5/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01048626
VIA PAD GEOMETRY SUPPORTING UNIFORM TRANSMISSION LINE STRUCTURES
VERBINDUNGSLOCHKONFIGURATIONZURUNTERSTUTZUNG EINER GLEICHMASSIGEN UBERTRAGUNGSLEITUNGSSTRUKTUR
CONFIGURATION DE PLAGES DE CONNEXION A TRAVERSEES SOUTENANT DES STRUCTURES DE LIGNES DE TRANSMISSION UNIFORMES
PATENT ASSIGNEE:
INTEL CORPORATION, (322933), 2200 Mission College Boulevard, Santa Clara, CA 95052, (US), (Applicant designated States: all)
INVENTOR:
LEDDIGE, Michael , 15820 S.W. Galena Way, Beaverton, OR 97007, (US)
SPRIETSMA, John, 860 S.W. 238, Hillsboro, OR 92123, (US
LEGAL REPRESENTATIVE:
Molyneaux, Martyn William et al (34019), Harrison Goddard Foote 40-43 Chancery Lane, London WC2A 1JA, (GB)
PATENT (CC, No, Kind, Date): EP 1029431 A1 000823 (Basic)
WO 9922552 990506

APPLICATION (CC, No, Date): EP 98943307 980820; WO 98US17397 980820
PRIORITY (CC, No, Date): US 959244 971028
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: H05K-007/02
NOTE:
No A-document published by EPO
LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	000823	A1	Published application with search report
Application:	990707	A1	International application (Art. 158(1))
Change:	040303	A1	Legal representative(s) changed 20040116
Change:	020724	A1	International Patent Classification changed: 20020603
Change:	020724	A1	International Patent Classification changed: 20020603
Search Report:	020724	A1	Date of drawing up and dispatch of supplementary:search report 20020607
Examination:	000823	A1	Date of request for examination: 20000526
Change:	010905	A1	Legal representative(s) changed 20010718
Examination:	040107	A1	Date of dispatch of the first examination report: 20031114

LANGUAGE (Publication,Procedural,Application): English; English; English

3/5/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00717314
Optical device heat spreader and thermal isolation apparatus.
Einrichtung zur Warmeableitung und zur thermischen Isolierung einer optischen Baugruppe.
Appareil pour la dissipation de la chaleur et pour l'isolation thermique d'un dispositif optique.
PATENT ASSIGNEE:
INTERNATIONAL BUSINESS MACHINES CORPORATION, (200123), , Armonk, NY 10504, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Block, Timothy R., 4516 Avon Lane, NW, Rochester, MN 55901, (US)
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Leddige, Michael W. , 1734 Fox Valley Drive, SW, Rochester, MN 55902, (US
LEGAL REPRESENTATIVE:
de Pena, Alain et al (15151), Compagnie IBM France Departement de Propriete Intellectuelle, 06610 La Gaude, (FR)
PATENT (CC, No, Kind, Date): EP 678765 A1 951025 (Basic)
APPLICATION (CC, No, Date): EP 95480010 950221;
PRIORITY (CC, No, Date): US 228972 940418
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G02B-006/42;

ABSTRACT EP 678765 A1
Attachment of electronics to optical devices is made by supporting the optical devices on a heat spreader card (12) and the electronics on a separate circuit card (16). Each card has at least a first major surface, with an optical transducing sub-assembly (14) mounted perpendicularly from the major surface of the heat spreader card (12). Electronics (18,20), except for transducing elements, are placed on the circuit card (16). The only direct attachment between the circuit card and the heat spreader card is one or more flexible cables (22) attached to the respective major surfaces. This arrangement mechanically isolates the circuit card (16) from the heat spreader card (12). The flexible cables (22) include electrical conductors held positionally in a polyimide matrix, which provides for thermal isolation of the heat spreader card and the circuit card. (see image in original document)

ABSTRACT WORD COUNT: 172

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 951025 A1 Published application (Alwith Search Report ;A2without Search Report)
Examination: 960410 A1 Date of filing of request for examination: 960213
Examination: 960529 A1 Date of despatch of first examination report: 960412
Change: 970319 A1 Representative (change)
Withdrawal: 990120 A1 Date on which the European patent application was deemed to be withdrawn: 980721
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB95	323
SPEC A	(English)	EPAB95	1734
Total word count - document A			2057
Total word count - document B			0
Total word count - documents A + B			2057

3/5/4 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00504334 **Image available**
A VERTICAL CONNECTOR BASED PACKAGING SOLUTION FOR INTEGRATED CIRCUITS
PROCEDE DE CONDITIONNEMENT UTILISANT DES CONNECTEURS VERTICAUX POUR CIRCUITS INTEGRES
Patent Applicant/Assignee:
INTEL CORPORATION,
HOLMAN Thomas J,
LEDDIGE Michael W,
Inventor(s):
HOLMAN Thomas J,
LEDDIGE Michael W
Patent and Priority Information (Country, Number, Date):
Patent: WO 9935686 A1 19990715
Application: WO 98US27517 19981221 (PCT/WO US9827517)
Priority Application: US 982775 19980105
Designated States: AL AM AT AT AU AZ BA BB BG BR BY CA CH CN CU CZ CZ DE DE DK DK EE EE ES FI FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SK SL TJ TM TR TT UA UG US UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Main International Patent Class: H01L-023/02
International Patent Class: H01L-023/043; H01L-023/047; H01L-023/053; H01L-023/057; H01L-023/12; H05K-001/11; H05K-001/14; H05K-007/02; H05K-007/06; H05K-007/20
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 4137

English Abstract
An assembly featuring a substrate (940) and a plurality of components (900). The plurality of components are packaged to be connected in a vertical orientation to the substrate. These components include (i) a vertical chip scale package (CSP), (ii) an integrated circuit die (930) and (iii) an interconnect (950). Including a plurality of connection leads, the vertical CSP contains the die which is generally situated along a vertical plane. The interconnect, capable of transferring information between the plurality of connection leads and the integrated circuit die, includes a first segment generally perpendicular to the

vertical plane and connected to at least one connection lead. The interconnect further includes a second segment generally in parallel to the vertical plane and connected to the integrated circuit die.

French Abstract
Ensemble presentant un substrat (940) et une pluralite (900) de composants. Les composants sont conditionnes de maniere a etre connectes au substrat en etant orientes verticalement. Ces composants comprennent (i) un boitier vertical de la taille d'une puce (CSP), (ii) une puce (930) de circuit integre et (iii) une interconnexion (950). Y compris une pluralite de fils de connexion, le CSP vertical contient la puce qui est generalement situee le long d'un plan vertical. L'interconnexion, capable de transmettre des informations entre la pluralite de fils de connexion et la puce de circuit integre, comprend un premier segment generalement perpendiculaire au plan vertical et connecte a au moins un fil de connexion. L'interconnexion comprend en outre un deuxieme segment generalement parallele au plan vertical et connecte a la puce de circuit integre.

3/5/5 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00491200 **Image available**
VIA PAD GEOMETRY SUPPORTING UNIFORM TRANSMISSION LINE STRUCTURES
CONFIGURATION DE PLAGES DE CONNEXION A TRAVERSEES SOUTENANT DES STRUCTURES DE LIGNES DE TRANSMISSION UNIFORMES
Patent Applicant/Assignee:
INTEL CORPORATION,
LEDDIGE Michael,
SPRIETSMA John,
Inventor(s):
LEDDIGE Michael ,
SPRIETSMA John
Patent and Priority Information (Country, Number, Date):
Patent: WO 9922552 A1 19990506
Application: WO 98US17397 19980820 (PCT/WO US9817397)
Priority Application: US 97959244 19971028
Designated States: AL AM AT AT AU AZ BA BB BG BR BY CA CH CN CU CZ CZ DE DE DK DK EE EE ES FI FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SK SL TJ TM TR TT UA UG US UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Main International Patent Class: H05K-007/02
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 3933

English Abstract
A connector (400) for coupling high frequency signals between devices includes a substrate having an array of vias (410) for coupling a reference voltage to reference voltages traces (460) that extend along the substrate surface between the devices. Signal traces (430) including device pads (434) for coupling signals to and from the devices alternate with the reference voltage traces (460). The widths of the reference voltage traces (460) are varied to maintain a substantially constant separation between the reference voltage trace (460) and an adjacent signal trace (430).

French Abstract
Ce connecteur (400) destine au passage de signaux haute frequence entre des dispositifs comprend un substrat porteur d'un reseau de traversees (310) servant au couplage d'une tension de reference a des traces

conducteurs (460) s'etendant sur toute la surface du substrat entre les dispositifs susmentionnes. Les traces conducteurs de signal (430), qui comprennent des plages de connexion de dispositifs (434) servant au passage de signaux en direction dispositifs et en provenance de ceux-ci, alternent avec les traces conducteurs de tension de reference (460). La largeur des traces conducteurs de tension de reference (460) varie afin que soit maintenu sensiblement constant l'intervalle separant un trace conducteur de tension de reference (460) du trace conducteur de signal (430) adjacent.

3/5/6 (Item 1 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015813759 **Image available**
WPI Acc No: 2003-875963/200381
XRPX Acc No: N03-699481

Single-ended memory interface system for personal computer, includes control interface and memory interfaces which are connected to separate power supplies, are coupled directly

Patent Assignee: MCCALL J A (MCCA-I); TO H Y (TOHY-I)
Inventor: **MCCALL J A** ; TO H Y
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030208668	A1	20031106	US 2002138540	A	20020502	200381	B

Priority Applications (No Type Date): US 2002138540 A 20020502
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030208668	A1		18	G06F-012/00	

Abstract (Basic): US 20030208668 A1

NOVELTY - Several single-ended memory interfaces (108) are coupled directly to a control interface (104). The control and memory interfaces connected to separate power supplies (110,112), are configured to drive respective output signals. The output signals are transmitted to a common supply (114) that is connected to both interfaces, to transfer a logic low.

USE - For communication between personal computer, workstations.

ADVANTAGE - Provides an optimal and efficient data transfer between control unit and memory units. Eliminates performance compromises in each interface by providing separate power supplies to control and memory interfaces.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic view of the memory interface system.

control interface (104)
memory interfaces (108)
power supplies (110,112)
common supply (114)
bus (120)
pp; 18 DwgNo 1/11

Title Terms: SINGLE; END; MEMORY; INTERFACE; SYSTEM; PERSON; COMPUTER; CONTROL; INTERFACE; MEMORY; INTERFACE; CONNECT; SEPARATE; POWER; SUPPLY; COUPLE
Derwent Class: T01
International Patent Class (Main): G06F-012/00
File Segment: EPI

3/5/7 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015813580 **Image available**
WPI Acc No: 2003-875784/200381

XRPX Acc No: N03-699[illegible]

Differential memory interface system for personal computer, operates differential control interface buffer unit with lower voltage power supply than that of single ended memory interfaces

Patent Assignee: MCCALL J A (MCCA-I); TO H Y (TOHY-I)
Inventor: **MCCALL J A** ; TO H Y
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030206046	A1	20031106	US 2002136920	A	20020501	200381	B

Priority Applications (No Type Date): US 2002136920 A 20020501
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030206046	A1		19	H03L-005/00	

Abstract (Basic): US 20030206046 A1

NOVELTY - A differential control interface that drives the differential output control signal and multiple single end memory interfaces (108) are connected through a buffer unit such that the differential control interface (104) and buffer unit (140) are operated with a lower voltage power supply (114) than the power supply (118) of the single-ended memory interfaces.

USE - For personal computers and workstations.

ADVANTAGE - Operates at higher frequencies because two signal are used to transfer one piece of data resulting in higher overall signal integrity. The differential interface provides optional and efficient data transfer.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic view of the memory interface system.

memory interface system (100)
control unit (102)
control interface (104)
memory units (106)
memory interface (108)
control interface power supply (110)
memory module (112)
memory control hub (130)
buffer unit (140)
pp; 19 DwgNo 1/11

Title Terms: DIFFERENTIAL; MEMORY; INTERFACE; SYSTEM; PERSON; COMPUTER; OPERATE; DIFFERENTIAL; CONTROL; INTERFACE; BUFFER; UNIT; LOWER; VOLTAGE; POWER; SUPPLY; SINGLE; END; MEMORY; INTERFACE
Derwent Class: T01; U14
International Patent Class (Main): H03L-005/00
File Segment: EPI

3/5/8 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015599051 **Image available**
WPI Acc No: 2003-661206/200362
XRPX Acc No: N03-527488

Memory controller for computer motherboards, has delay adjustment circuitry to receive signals regarding relative delays and select amongst taps to achieve relative delays between clock and data signals

Patent Assignee: MCCALL J A (MCCA-I); TO H Y (TOHY-I); INTEL CORP (ITLC)
Inventor: **MCCALL J A** ; TO H Y
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030122583	A1	20030703	US 200139438	A	20011228	200362	B
US 6597202	B1	20030722	US 200139438	A	20011228	200362	

Priority Applications (No Type Date): US 200139438 A 20011228

Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
US 20030122583 A1   13 H03K-019/96
US 6597202   B1   H03K-019/00

Abstract (Basic): US 20030122583 A1
NOVELTY - The controller (104) has multiphase producing circuitry with multiple taps to receive a clock signal that produces phases on taps. A delay determining circuitry (110) with lookup table determines the relative delay between clock and data signals. A delay adjustment circuitry (114) receives the signals corresponding to relative delay and selects the taps to achieve the relative delay between clock and data signals.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a system with skew control.
USE - Used for controlling memory modules in computer motherboards.

ADVANTAGE - The controller provides a delay to clock or data signals thereby the signals are properly aligned when received by clocked receiver.
DESCRIPTION OF DRAWING(S) - The drawing shows a schematic representation of a system with a controller.
Controller (104)
Delay determining circuitry (110)
Delay adjustment circuitry. (114)
pp; 13 DwgNo 5/9
Title Terms: MEMORY; CONTROL; COMPUTER; DELAY; ADJUST; CIRCUIT; RECEIVE; SIGNAL; RELATIVE; DELAY; SELECT; TAP; ACHIEVE; RELATIVE; DELAY; CLOCK; DATA; SIGNAL
Derwent Class: T01; U22; U23
International Patent Class (Main): H03K-019/00; H03K-019/96
File Segment: EPI

3/5/9 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015598120 **Image available**
WPI Acc No: 2003-660275/200362
XRPX Acc No: N03-526563
Impedance compensation system for printed circuit board, has low impedance package trace compensation section positioned closer to high impedance matching region trace section in PCB break-out region
Patent Assignee: MCCALL J A (MCCA-I); SHYKIND D N (SHYK-I); STAHLBERG S M (STAH-I); INTEL CORP (ITLC)
Inventor: **MCCALL J A** ; SHYKIND D N; STAHLBERG S M
Number of Countries: 001 Number of Patents: 002
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 20030116831 A1 20030626 US 200133831 A 20011226 200362 B
US 6700457 B2 20040302 US 200133831 A 20011226 200417

Priority Applications (No Type Date): US 200133831 A 20011226
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
US 20030116831 A1   12 H01L-023/495
US 6700457   B2   H03H-007/38
Abstract (Basic): US 20030116831 A1
NOVELTY - The low impedance package trace compensation sections (72A-72D) are positioned closer to the high impedance matching region trace sections (66A-66D), such that their effective impedance is approximately equal to the impedance of fan-out trace sections (40) in the PCB break-out region (62) of an impedance matching region (80).
USE - For impedance compensation in circuit board break-out regions of printed circuit boards (PCBs).
ADVANTAGE - Cross-talks and unwanted reflections which lower

switching speed of signal, are reduced.
DESCRIPTION OF DRAWING(S) - The figure shows a schematic plan view of impedance compensation system.
fan-out trace sections (40)
PCB break-out region (62)
high impedance matching region trace sections (66)
low impedance package trace compensation sections (72)
matching region (80)
pp; 12 DwgNo 2/13
Title Terms: IMPEDANCE; COMPENSATE; SYSTEM; PRINT; CIRCUIT; BOARD; LOW; IMPEDANCE; PACKAGE; TRACE; COMPENSATE; SECTION; POSITION; CLOSE; HIGH; IMPEDANCE; MATCH; REGION; TRACE; SECTION; PCB; BREAK; REGION
Derwent Class: V04
International Patent Class (Main): H01L-023/495; H03H-007/38
File Segment: EPI

3/5/10 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015582026 **Image available**
WPI Acc No: 2003-644183/200361
XRPX Acc No: N03-512387
Memory channel continuity module for computer system, has capacitive load comprising sub-traces oriented perpendicular to signal traces having thin, thick sections of printed circuit board
Patent Assignee: INTEL CORP (ITLC)
Inventor: **LEDDIGE M W ; MCCALL J A**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6539449	B1	20030325	US 2000524850	A	20000314	200361	B

Priority Applications (No Type Date): US 2000524850 A 20000314
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6539449	B1		6	G06F-013/00	

Abstract (Basic): US 6539449 B1
NOVELTY - A printed circuit board (PCB) (115) coupled to an interconnector (103) of a motherboard (100), has signal traces (112) having relative thin and thick sections (106,107). A capacitive load has sub-traces (113) that are oriented perpendicular to the signal traces (112).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a computer system.
USE - For computer system (claimed).
ADVANTAGE - By adding a capacitive load to the traces formed on the continuity module, edge rates of signals at certain frequencies are made low, and hence crosstalk between adjacent traces are reduced. Adding capacitance to system, dampens the channel, thus ensuring proper performance of systems with small number of memory devices.
DESCRIPTION OF DRAWING(S) - The figure shows the schematic view of a computer system.
mother board(103) interconnect (100)
relatively thin section (106)
relatively thick section (107)
memory module (110)
continuity module (111)
signal trace (112)
sub-trace (113)
PCB (115)
pp; 6 DwgNo 4/4
Title Terms: MEMORY; CHANNEL; CONTINUE; MODULE; COMPUTER; SYSTEM; CAPACITANCE; LOAD; COMPRISE; SUB; TRACE; ORIENT; PERPENDICULAR; SIGNAL; TRACE; THIN; THICK; SECTION; PRINT; CIRCUIT; BOARD

Derwent Class: T01; V0
International Patent Class (Main): G06F-013/00
File Segment: EPI

3/5/11 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015493422 **Image available**
WPI Acc No: 2003-555569/200352
XRPX Acc No: N03-441263
Multi-level coding method e.g. for digital communication through computer bus, involves combining input digital signal or analog signal with delayed input signal by predetermined operation
Patent Assignee: INTEL CORP (ITLC)
Inventor: HECK H L; **LEDDIGE M W** ; MIX J A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030063677	A1	20030403	US 2001968641	A	20010928	200352	B

Priority Applications (No Type Date): US 2001968641 A 20010928
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030063677	A1		11	H04L-027/00	

Abstract (Basic): US 20030063677 A1
NOVELTY - The input digital signal or analog signal is delayed for predetermined minimum bit period. The input digital signal or analog signal is combined with the delayed input signal by an operation selected from the group containing modulo 2 binary addition, a modulo 2 binary subtraction, an exclusive-OR logic function, a digital adder, an analog adder and a mixer.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(1) multi-level coding apparatus;
(2) computer readable medium storing multi-level coding program;
(3) processor system memory interface;
(4) N-level encoding method;
(5) N-level decoding method;
(6) computer readable medium storing N-level encoding program; and
(7) computer readable medium storing N-level decoding program.
USE - For multi-level coding for communication of data for transfer through computer bus between computer components such as memories, disk drives, processors. Also for digital communications in distributed network environment using satellite link, cable network, Internet, wide area network (WAN), local area network (LAN), high speed busses, on-chip paths. Also for multi-level coding using computer system including handheld device, multiprocessor system, microprocessor-based or programmable consumer electronics, digital signal processor (DSP), minicomputer, mainframe computer, data communication. Also using bus switches, routers and other networking devices.
ADVANTAGE - Allows easy multi-level coding without causing distortion by using simple circuit configuration.
DESCRIPTION OF DRAWING(S) - The figure depicts a flowchart illustrating steps involved in duo-binary encoding.
pp; 11 DwgNo 4/7
Title Terms: MULTI; LEVEL; CODE; METHOD; DIGITAL; COMMUNICATE; THROUGH; COMPUTER; BUS; COMBINATION; INPUT; DIGITAL; SIGNAL; ANALOGUE; SIGNAL; DELAY; INPUT; SIGNAL; PREDETERMINED; OPERATE
Derwent Class: T01; U21; W01
International Patent Class (Main): H04L-027/00
File Segment: EPI

3/5/12 (Item 7 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015477966 **Image available**
WPI Acc No: 2003-540113/200351
XRPX Acc No: N03-428335

Semiconductor chip module e.g. in-line memory modules has circuit board having module connectors to receive two modules with two clock paths of conductors to carry signals to chips

Patent Assignee: LEDDIGE M W (LEDD-I); MCCALL J A (MCCA-I); TO H Y (TOHY-I); INTEL CORP (ITLC)
Inventor: **LEDDIGE M W ; MCCALL J A ;** TO H Y
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030016549	A1	20030123	US 2001911756	A	20010723	200351	B
US 6631083	B2	20031007	US 2001911756	A	20010723	200374	

Priority Applications (No Type Date): US 2001911756 A 20010723
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030016549	A1		39	G11C-005/02	
US 6631083	B2			G11C-005/02	

Abstract (Basic): US 20030016549 A1

NOVELTY - A circuit board (12) includes respective connectors (20,22) to receive two modules. A first clock path of conductors to carry a first clock signal to four chips on the first module and then to the four chips on the second module. A second clock path of conductors carries a second clock signal to the four chips on the second module and then to the four chips on the first module.

USE - Semiconductor chip module e.g. single in-line memory module (SIMM), dual in-line memory module (DIMM).

ADVANTAGE - The system uses on-module terminations, to reduce the number of connector connections, connector contacts and corresponding fingers by a factor of 1/4. The module and module slots are keyed to prevent the modules being inserted into the slots in the wrong orientation.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic plan view of a system including motherboard, controller and two module connectors.

circuit board (12)
module connectors (20,22)
pp; 39 DwgNo 1/39

Title Terms: SEMICONDUCTOR; CHIP; MODULE; LINE; MEMORY; MODULE; CIRCUIT; BOARD; MODULE; CONNECT; RECEIVE; TWO; MODULE; TWO; CLOCK; PATH; CONDUCTOR ; CARRY; SIGNAL; CHIP
Derwent Class: T01; U14; V04
International Patent Class (Main): G11C-005/02
File Segment: EPI

3/5/13 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015469429 **Image available**
WPI Acc No: 2003-531575/200350
XRPX Acc No: N03-421734

Dynamic setting of driver output impedance for chipset drivers, involves setting chipset driver output impedance based on detected system memory configuration to increase interconnect timing budget

Patent Assignee: LEDDIGE M W (LEDD-I); MCCALL J A (MCCA-I); STAHLBERG S M (STAH-I)
Inventor: **LEDDIGE M W ; MCCALL J A ;** STAHLBERG S M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week

US 20030056128 A1 20030320 US 2001957104 A 20010920 200350 B

Priority Applications (No Type Date): US 2001957104 A 20010920
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20030056128 A1 18 G06F-001/26

Abstract (Basic): US 20030056128 A1
NOVELTY - The method involves detecting a system memory configuration. A chipset driver output impedance is set according to the detected system memory configuration, thereby increasing the interconnect timing budget.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(a) the computer-readable storage medium storing instructions for dynamic setting of driver output impedance for chipset drivers;
(b) the dynamic setting apparatus for driver output impedance for chipset drivers; and
(c) the electronic system.
USE - For chipset drivers.
ADVANTAGE - Avoids voltage swings, as well as reflections, along the memory bus transmission lines. Ensures effective reduction in the amount of time required for signal to propagate along memory bus from chipset driver to actual memory device, thus increasing total interconnect timing budget. Can be performed by specific hardware components that contain hardwired logic for performing steps or by any combination of programmed computer components and custom hardware components. Allows future design to incorporate increased clock speeds due to reduced interconnect time.
DESCRIPTION OF DRAWING(S) - The figure is a block diagram showing the computer system for dynamic setting of driver output impedance for chipset drivers.
pp; 18 DwgNo 4/12
Title Terms: DYNAMIC; SET; DRIVE; OUTPUT; IMPEDANCE; DRIVE; SET; DRIVE; OUTPUT; IMPEDANCE; BASED; DETECT; SYSTEM; MEMORY; CONFIGURATION; INCREASE ; INTERCONNECT; TIME; BUDGET
Derwent Class: T01
International Patent Class (Main): G06F-001/26
File Segment: EPI

3/5/14 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015403919 **Image available**
WPI Acc No: 2003-466059/200344
Related WPI Acc No: 2003-289064; 2003-330843; 2003-341550
XRPX Acc No: N03-370713
Semiconductor chip module connection system has two groups of conductor paths each having short loop through section which couples with modules through stubs
Patent Assignee: LEDDIGE M W (LEDD-I); MCCALL J A (MCCA-I)
Inventor: **LEDDIGE M W ; MCCALL J A**
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 20030018940 A1 20030123 US 2001911634 A 20010723 200344 B

Priority Applications (No Type Date): US 2001911634 A 20010723
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20030018940 A1 37 H03M-013/00

Abstract (Basic): US 20030018940 A1
NOVELTY - Two group of conductor paths extend from the circuit board (12) comprising several connectors (20,22), to the semiconductor

chip modules. Each group has a short loop through section which couples with the modules through stubs.

USE - For connecting semiconductor chip modules such as single inline memory modules (SIMMs), dual inline memory modules (DIMMs) used in SDRAM.

ADVANTAGE - Reduces the number of connectors.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic plan view of the circuit board.

circuit board (12)

connectors (20,22)

pp; 37 DwgNo 2/39

Title Terms: SEMICONDUCTOR; CHIP; MODULE; CONNECT; SYSTEM; TWO; GROUP; CONDUCTOR; PATH; SHORT; LOOP; THROUGH; SECTION; COUPLE; MODULE; THROUGH; STUB

Derwent Class: T01; U11; U14

International Patent Class (Main): H03M-013/00

File Segment: EPI

3/5/15 (Item 10 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015280619 **Image available**

WPI Acc No: 2003-341550/200332

Related WPI Acc No: 2003-289064; 2003-330843; 2003-466059

XRPX Acc No: N03-273220

Semiconductor chip module for motherboard of computer, includes first and second group of chips that are coupled to the corresponding group of conductors

Patent Assignee: MCCALL J A (MCCA-I); TO H Y (TOHY-I)

Inventor: **MCCALL J A** ; TO H Y

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030015346	A1	20030123	US 2001911634	A	20010723	200332 B
			US 2001911635	A	20010723	
			US 2001971947	A	20011004	

Priority Applications (No Type Date): US 2001971947 A 20011004; US 2001911634 A 20010723; US 2001911635 A 20010723

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030015346	A1		43	H05K-001/16	CIP of application US 2001911634 CIP of application US 2001911635

Abstract (Basic): US 20030015346 A1

NOVELTY - A first and second group of chips (11-18,110-116) are coupled to the corresponding group of conductors. The second group of conductors have higher impedances than the first group of conductors.

USE - For motherboard of computer.

ADVANTAGE - Reduces impedance mismatch. Higher impedance values can be higher or lower depending on physical layer PCB routing feasibility. Module termination external from the die does not have to be added to the die, thus reducing silicon thermal junction temperature risk.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic plan view of the motherboard.

Chips (11-18,110-116)

pp; 43 DwgNo 12/47

Title Terms: SEMICONDUCTOR; CHIP; MODULE; COMPUTER; FIRST; SECOND; GROUP; CHIP; COUPLE; CORRESPOND; GROUP; CONDUCTOR

Derwent Class: T01; U25; V04

International Patent Class (Main): H05K-001/16

File Segment: EPI

3/5/16 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX
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015269917 **Image available**
WPI Acc No: 2003-330846/200331
XRPX Acc No: N03-264950

Termination card for semiconductor memory modules, has substrates with multiple fingers which are selectively connected through module connectors, provided on either sides

Patent Assignee: HORINE B D (HORI-I); MCCALL J A (MCCA-I); Y TO H T (TOHT-I); INTEL CORP (ITLC)
Inventor: HORINE B D; **MCCALL J A** ; TO H T Y
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030016516	A1	20030123	US 2001911754	A	20010723	200331	B
US 6674648	B2	20040106	US 2001911754	A	20010723	200411	

Priority Applications (No Type Date): US 2001911754 A 20010723
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030016516	A1		39	H05K-007/06	
US 6674648	B2			H05K-007/06	

Abstract (Basic): US 20030016516 A1

NOVELTY - The termination card has a substrate with multiple fingers provided on either sides. The fingers on either sides are selectively connected through module connectors, and the other fingers are connected to module terminations on respective sides.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for termination system.

USE - Termination card for semiconductor memory modules e.g. single in line memory modules (SIMMs), dual in line memory modules (DIMMs), double data rate (DDR) SDRAM, etc., used in computer.

ADVANTAGE - Enhances reliability and simplifies interconnection between adjacent modules.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional side view of the termination system.

pp; 39 DwgNo 30/39

Title Terms: TERMINATE; CARD; SEMICONDUCTOR; MEMORY; MODULE; SUBSTRATE; MULTIPLE; FINGER; SELECT; CONNECT; THROUGH; MODULE; CONNECT; SIDE
Derwent Class: T01; U11; U14; V04
International Patent Class (Main): H05K-007/06
File Segment: EPI

3/5/17 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

015269916 **Image available**
WPI Acc No: 2003-330845/200331
XRPX Acc No: N03-264949

Semiconductor chip module connection system has circuit board with conductor paths each of which is looped between connectors and associated module and terminated at other module

Patent Assignee: INTEL CORP (ITLC); MCCALL J A (MCCA-I); Y TO H T (TOHT-I)
Inventor: **MCCALL J A** ; TO H T Y
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030016514	A1	20030123	US 2001911760	A	20010723	200331	B
US 6674649	B2	20040106	US 2001911760	A	20010723	200411	
TW 550986	A	20030901	TW 2002116243	A	20020722	200413	

Priority Applications (No Type Date): US 2001911760 A 20010723
Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes
US 20030016514 A1 39 H05K-001/11
US 6674649 B2 H05K-007/06
TW 550986 A H05K-001/00

Abstract (Basic): US 20030016514 A1
NOVELTY - A circuit board includes module connectors (116,118) and modules (1,2). Each of the conductor paths (8,7) extending from the circuit board, is looped between the connectors and associated module and terminated at other module
USE - For connecting semiconductor chip modules such as memory module including single in-line memory module (SIMM) and dual in-line memory module (DIMM).
ADVANTAGE - By using module termination, the number of connector connections and connector contact are reduced to a factor of 1/4, thereby high speed signaling is achieved.
DESCRIPTION OF DRAWING(S) - The figure shows the layout of connection between the semiconductor modules.
modules (1,2)
conductor paths (7,8)
module connectors (116,118)
pp; 39 DwgNo 15/39
Title Terms: SEMICONDUCTOR; CHIP; MODULE; CONNECT; SYSTEM; CIRCUIT; BOARD; CONDUCTOR; PATH; LOOP; CONNECT; ASSOCIATE; MODULE; TERMINATE; MODULE
Derwent Class: T01; U14; V04
International Patent Class (Main): H05K-001/00; H05K-001/11; H05K-007/06
International Patent Class (Additional): H01R-012/16
File Segment: EPI

3/5/18 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015269915 **Image available**
WPI Acc No: 2003-330844/200331
XRPX Acc No: N03-264948
Multi-modular system e.g. for single inline memory module, has primary section which is divided into two different sections which provides impedance greater than primary sections
Patent Assignee: MCCALL J A (MCCA-I); TO H T Y (TOHT-I)
Inventor: **MCCALL J A** ; TO H T Y
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 20030016513 A1 20030123 US 2001911752 A 20010723 200331 B

Priority Applications (No Type Date): US 2001911752 A 20010723
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20030016513 A1 39 H05K-007/10

Abstract (Basic): US 20030016513 A1
NOVELTY - A circuit board has module connectors to receive respective modules (1,2) having group of chips (18). A pair of buffers provides signals received from respective sections of the paths (7,8) to the group of chips. The path has conductors in a primary section that is divided into two different sections which provides an impedance of 50% greater than the primary section.
USE - For memory modules such as single inline memory module (SIMM) and dual inline memory module (DIMM).
ADVANTAGE - Prevents incorrect insertion of modules, by having keyed module slots. Decouples the receiver voltage supply from the driver voltage supply.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional side view of multi-modular system.
modules (1,2)

paths (7,8)
chip (18)
pp; 39 DwgNo 15/39
Title Terms: MULTI; MODULE; SYSTEM; SINGLE; MEMORY; MODULE; PRIMARY; SECTION; DIVIDE; TWO; SECTION; IMPEDANCE; GREATER; PRIMARY; SECTION
Derwent Class: T01; U14; V04
International Patent Class (Main): H05K-007/10
File Segment: EPI

3/5/19 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015269914 **Image available**
WPI Acc No: 2003-330843/200331
Related WPI Acc No: 2003-289064; 2003-341550
XRPX Acc No: N03-264947

Semiconductor chip module e.g. synchronous dynamic random access memory module has die terminations in chips which are respectively disabled and enabled

Patent Assignee: LEDDIGE M W (LEDD-I); MCCALL J A (MCCA-I); TO H Y (TOHY-I)
Inventor: **LEDDIGE M W** ; **MCCALL J A** ; TO H Y
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030016512	A1	20030123	US 2001911635	A	20010723	200331	B

Priority Applications (No Type Date): US 2001911635 A 20010723
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030016512	A1		37	H05K-001/11	

Abstract (Basic): US 20030016512 A1
NOVELTY - The paths (8,7) in the modules (1,2) are coupled to respective stubs (140,142 and 144,146) of the chips (I8,I16) of the modules. The die terminations of the chips of modules are disabled and enabled, respectively.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for dynamic random access memory.
USE - E.g. single inline memory module, dual inline memory of synchronous dynamic random access memory (SDRAM), double data rate (DDR) SDRAM.
ADVANTAGE - Since the termination of the module external to the die, does not have to be added to the die, the silicon thermal junction temperature risk can be reduced, at low cost. By reducing the impedance ratio of the node and ground, the matching, during the voltage swing for equivalent driver current, can be improved.
DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional side view of the semiconductor chip module.
modules (1,2)
paths (8,7)
stubs (140,142 and 144,146)
chips (I8,I16)
pp; 37 DwgNo 15/39
Title Terms: SEMICONDUCTOR; CHIP; MODULE; SYNCHRONOUS; DYNAMIC; RANDOM; ACCESS; MEMORY; MODULE; DIE; TERMINATE; CHIP; RESPECTIVE; DISABLE; ENABLE
Derwent Class: T01; U11; U14; V04
International Patent Class (Main): H05K-001/11
International Patent Class (Additional): H01R-012/16
File Segment: EPI

3/5/20 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015228151 **Image available**
WPI Acc No: 2003-289064/200328
Related WPI Acc No: 2003-330843; 2003-341550; 2003-466059
XRPX Acc No: N03-229888

Paths layout system for circuit board and module, has pair of modules consists of chips among which chips of either one module has enabled on die terminations

Patent Assignee: MCCALL J A (MCCA-I); TO H Y (TOHY-I)
Inventor: **MCCALL J A** ; TO H Y
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030016517	A1	20030123	US 2001911634	A	20010723	200328	B
			US 2001911635	A	20010723		
			US 2001970442	A	20011004		

Priority Applications (No Type Date): US 2001970442 A 20011004; US 2001911634 A 20010723; US 2001911635 A 20010723
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030016517	A1		43	G11C-005/06	CIP of application US 2001911634 CIP of application US 2001911635

Abstract (Basic): US 20030016517 A1

NOVELTY - The paths (7,8) are coupled to chips (I8,I16) of respective modules (2,1). The chips of either one module includes enabled on die terminations.

USE - For circuit boards and modules.

ADVANTAGE - Reduces impedance mismatch. Higher impedance values are higher or lower, depending on physical layer PCB routing feasibility.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional side view of the paths layout system.

modules (1,2)
paths (7,8)
chips (I8,I16)
pp; 43 DwgNo 15/47

Title Terms: PATH; LAYOUT; SYSTEM; CIRCUIT; BOARD; MODULE; PAIR; MODULE; CONSIST; CHIP; CHIP; ONE; MODULE; ENABLE; DIE; TERMINATE
Derwent Class: U11; V04
International Patent Class (Main): G11C-005/06
International Patent Class (Additional): H05K-001/11
File Segment: EPI

3/5/21 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015030004 **Image available**
WPI Acc No: 2003-090521/200308
XRPX Acc No: N03-071497

Increased data transfer rate system for digital computer system, encodes every buffered three bits of signal waveform and produces encoded waveform containing three bits of information for each bit time of waveform

Patent Assignee: HALL S H (HALL-I); LEDDIGE M W (LEDD-I)
Inventor: HALL S H; **LEDDIGE M W**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020131518	A1	20020919	US 2001810576	A	20010319	200308	B

Priority Applications (No Type Date): US 2001810576 A 20010319
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020131518	A1		11	H04L-027/04	

Abstract (Basic): US 20020131518 A1

NOVELTY - A buffer (12) receives a digital signal waveform containing one bit of information for every bit time of the waveform, and buffers every three bits of the waveform. An encoder (14) encodes every buffered three bits and produces an encoded waveform that contains three bits of information for each bit time of the digital signal waveform.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Data transfer rate increasing method;

(2) Encoding method; and

(3) Decoding method.

USE - For increasing data transfer rate in digital high speed systems.

ADVANTAGE - The encoder increases the data rate of digital waveforms without dramatically increasing the frequency content of the waveforms, thereby minimizing distortion.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of increased data transfer rate system.

Buffer (12)

Encoder (14)

pp; 11 DwgNo 2/5

Title Terms: INCREASE; DATA; TRANSFER; RATE; SYSTEM; DIGITAL; COMPUTER; SYSTEM; ENCODE; BUFFER; THREE; BIT; SIGNAL; WAVEFORM; PRODUCE; ENCODE; WAVEFORM; CONTAIN; THREE; BIT; INFORMATION; BIT; TIME; WAVEFORM

Derwent Class: T01; U21; W01

International Patent Class (Main): H04L-027/04

File Segment: EPI

3/5/22 (Item 17 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014911526 **Image available**

WPI Acc No: 2002-732232/200279

XRPX Acc No: N02-577381

Low weight data encoding circuit for power delivery system, encodes data bits and generates encoded data and corresponding decode bits, if preset number of data bits are not current balanced

Patent Assignee: HALL S H (HALL-I); LEDDIGE M W (LEDD-I)

Inventor: HALL S H; **LEDDIGE M W**

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020138805	A1	20020926	US 2001759245	A	20010116	200279	B

Priority Applications (No Type Date): US 2001759245 A 20010116

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020138805	A1		15	H03M-013/00	

Abstract (Basic): US 20020138805 A1

NOVELTY - A current balance encoder and decode bit generator generates encoded data and corresponding decode bits, if a preset number of data bits are not current balanced. A latch latches the data bits through an input/output bus, if the data bits are current balanced, and latches the encoded data and decode bits through the input/output bus, if the preset number of data bits are not current balanced.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Electronic system; and

(2) Data encoding method.

USE - For power delivery system and electronic device such as computer.

ADVANTAGE - Minimizes net current drawn from the local power

delivery system and the switching noise while eliminating the problems inherent with heavy decoupling and data-bus inversion techniques, so as to ensure signal integrity and minimize timing distortion. Decouples the active circuits, so as to adequately meet the power delivery demands of the input/output cells with minimal cost and space. Extends the life of non-differential high-speed bus technologies, and reduces risk by minimizing the timing uncertainty due to SSO effects.

DESCRIPTION OF DRAWING(S) - The figure shows the flow diagram of the power delivery system.

pp; 15 DwgNo 5/7

Title Terms: LOW; WEIGHT; DATA; ENCODE; CIRCUIT; POWER; DELIVER; SYSTEM; ENCODE; DATA; BIT; GENERATE; ENCODE; DATA; CORRESPOND; DECODE; BIT; PRESET; NUMBER; DATA; BIT; CURRENT; BALANCE

Derwent Class: T01; U21; U24

International Patent Class (Main): H03M-013/00

File Segment: EPI

3/5/23 (Item 18 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014762347 **Image available**

WPI Acc No: 2002-583051/200262

XRPX Acc No: N02-462415

Printed circuit board includes signal trace with primary section consisting pair of lines whose width is smaller than that of secondary section

Patent Assignee: LEDDIGE M W (LEDD-I); MCCALL J A (MCCA-I); INTEL CORP (ITLC)

Inventor: **LEDDIGE M W ; MCCALL J A**

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020079983	A1	20020627	US 2000746241	A	20001222	200262	B
US 6515555	B2	20030204	US 2000746241	A	20001222	200313	

Priority Applications (No Type Date): US 2000746241 A 20001222

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020079983	A1		7	H01P-003/08	
US 6515555	B2			H01P-003/08	

Abstract (Basic): US 20020079983 A1

NOVELTY - The capacitive load is coupled to the signal trace. The primary section of the signal trace is positioned between the capacitive load and a secondary section. The primary section has two lines, each having a width smaller than the width of secondary section.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Memory module; and

(2) Memory card.

USE - Printed circuit board (PCB).

ADVANTAGE - As the two lines have a width smaller than secondary section width, the space needed to install PCB is reduced.

DESCRIPTION OF DRAWING(S) - The figure shows an enlarged view of the printed circuit board.

pp; 7 DwgNo 2a/3

Title Terms: PRINT; CIRCUIT; BOARD; SIGNAL; TRACE; PRIMARY; SECTION; CONSIST; PAIR; LINE; WIDTH; SMALLER; SECONDARY; SECTION

Derwent Class: U14; V04

International Patent Class (Main): H01P-003/08

File Segment: EPI

3/5/24 (Item 19 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014716265 **Image available**
WPI Acc No: 2002-536969/200257
XRPX Acc No: N02-425270

Memory module in computer system, has signal trace with loaded portion whose sections are connected to input and output of DRAM such that impedance of loaded portion is high

Patent Assignee: LEDDIGE M W (LEDD-I); MCCALL J A (MCCA-I); INTEL CORP (ITLC)
Inventor: **LEDDIGE M W ; MCCALL J A**
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020073273	A1	20020613	US 2000734853	A	20001211	200257	B
US 6686762	B2	20040203	US 2000734853	A	20001211	200413	

Priority Applications (No Type Date): US 2000734853 A 20001211
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020073273	A1		5	G06F-012/00	
US 6686762	B2			H03K-017/16	

Abstract (Basic): US 20020073273 A1

NOVELTY - A signal trace (210) has unloaded and loaded portions. The loaded portion has two sections (270,280) respectively coupled to input and output connections (220,225) of a DRAM (260), such that the impedance of the loaded portion is higher than that when the two sections are coupled to the same connection of the DRAM.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Dynamic random access memory; and
(2) Memory card.

USE - E.g. memory card (claimed) used in computer system.

ADVANTAGE - Enables to closely match the impedance of the loaded portion of the signal trace to the impedance of the unloaded portion. Enhances signal integrity by not positioning the package inductance in series with the DRAM capacitance.

DESCRIPTION OF DRAWING(S) - The figure shows the memory card containing several DRAMs.

Signal trace (210)
Connections of DRAM (220,225)
DRAM (260)
Sections of loaded portions (270,280)
pp; 5 DwgNo 2B/2

Title Terms: MEMORY; MODULE; COMPUTER; SYSTEM; SIGNAL; TRACE; LOAD; PORTION ; SECTION; CONNECT; INPUT; OUTPUT; DRAM; IMPEDANCE; LOAD; PORTION; HIGH
Derwent Class: T01; U13
International Patent Class (Main): G06F-012/00; H03K-017/16
International Patent Class (Additional): H03K-019/003
File Segment: EPI

3/5/25 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014685661 **Image available**
WPI Acc No: 2002-506365/200254
XRPX Acc No: N02-400563

Multilayer PCB for motherboard assembly, connects signal traces using via such that thinner portion of particular trace is between thicker portion of trace and via

Patent Assignee: INTEL CORP (ITLC)
Inventor: HORINE B D; **LEDDIGE M W ; MCCALL J A**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6366466	B1	20020402	US 2000524450	A	20000314	200254	B

Priority Applications (No Type Date): US 2000524450 A 20000314
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 6366466 B1 9 H05K-001/02

Abstract (Basic): US 6366466 B1
NOVELTY - Signal traces (1,4) having thicker and thinner portions, are provided on upper, lower PCB layers (2,5) respectively. A via (9) connects the signal traces such that the thinner portion of the signal trace (1) is between the thicker portion of the trace (1) and the via.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for motherboard assembly.
USE - For motherboard assembly (claimed) and memory card.
ADVANTAGE - Enables signals to be passed from one PCB layer to another, through the via without generating any impedance discontinuities and at a reduced frequency.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the four-layer PCB.
Signal traces (1,4)
PCB layers (2,5)
Via (9)
pp; 9 DwgNo 1/5
Title Terms: MULTILAYER; PCB; ASSEMBLE; CONNECT; SIGNAL; TRACE; THINNER; PORTION; TRACE; THICK; PORTION; TRACE
Derwent Class: T01; V04
International Patent Class (Main): H05K-001/02
International Patent Class (Additional): H05K-001/14
File Segment: EPI

3/5/26 (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014677018 **Image available**
WPI Acc No: 2002-498075/200253
XRPX Acc No: N02-394149
Multi-layer printed circuit board has throttling member coupled to first signal trace to reduce speed at which first signal routed over first signal trace travels
Patent Assignee: INTEL CORP (ITLC)
Inventor: HORINE B D; **LEDDIGE M W**
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 6362973 B1 20020326 US 2000524627 A 20000314 200253 B

Priority Applications (No Type Date): US 2000524627 A 20000314
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 6362973 B1 6 H05K-001/02

Abstract (Basic): US 6362973 B1
NOVELTY - The printed circuit board includes a first layer and a second layer that have first and second signal traces (13,4), respectively. A signal transmitting component (10) is coupled by a via (9) to the second signal trace, and a throttling member is coupled to the first signal trace.
DETAILED DESCRIPTION - The throttling member reduces the speed at which a first signal routed over the first signal trace travels when compared to the speed at which same signal would have traveled had the throttling member been absent. An INDEPENDENT CLAIM is also included for a motherboard assembly.
USE - Multi-layer printed circuit board.
ADVANTAGE - Reduces skew between signals driven along PCB layer and signals driven along at least two PCB layers that are connected by a

via.

DESCRIPTION OF DRAWING(S) - The figures include a cross-section of a four-layer PCB that routes signals from a signal transmitting component located on one of the layers to a signal trace located on another layer, and an overhead view showing a signal trace, which routes signals between two components along a single PCB layer, coupled to a placebo via that has an oversized via pad.

Via (9)
Signal transmitting component (10)
Signal traces (13,4)
pp; 6 DwgNo 1/3

Title Terms: MULTI; LAYER; PRINT; CIRCUIT; BOARD; THROTTLE; MEMBER; COUPLE; FIRST; SIGNAL; TRACE; REDUCE; SPEED; FIRST; SIGNAL; ROUTE; FIRST; SIGNAL; TRACE; TRAVEL
Derwent Class: V04
International Patent Class (Main): H05K-001/02
International Patent Class (Additional): H05K-001/14
File Segment: EPI

3/5/27 (Item 22 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014604544 **Image available**
WPI Acc No: 2002-425248/200245
Related WPI Acc No: 2003-074646
XRPX Acc No: N02-334382

Memory module in computer system, has memory repeater hub connected to primary, secondary and tertiary buses

Patent Assignee: BONELLA R (BONE-I); HORINE B D (HORI-I); LEDDIGE M W (LEDD-I); MACWILLIAMS P D (MACW-I); INTEL CORP (ITLC)
Inventor: BONELLA R; HORINE B D; **LEDDIGE M W** ; MACWILLIAMS P D
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020038405	A1	20020328	US 98163860	A	19980930	200245	B
US 6587912	B2	20030701	US 98163860	A	19980930	200345	

Priority Applications (No Type Date): US 98163860 A 19980930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020038405	A1		15	G06F-013/00	
US 6587912	B2			G06F-012/00	

Abstract (Basic): US 20020038405 A1

NOVELTY - A memory module has a primary bus (300) connected to a memory repeater hub (320). Secondary and tertiary buses (321,322) are connected in series with the memory repeater hub. The memory hub routes signals either to secondary bus or tertiary bus, in response to address information received from primary bus.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Computer system; Signals routing method

USE - Memory module e.g. dual in-line memory module, single in-line memory module, dynamic random access memory module, synchronous dynamic random access memory module in computer system.

ADVANTAGE - Any number of memory repeater hubs can be implemented on a memory module to connect any number of additional memory buses to an existing memory bus for adding several memory devices. Thus the capacity of the memory system is increased and equal latency is provided.

DESCRIPTION OF DRAWING(S) - The figure shows the bus routing and writing topology for a memory system.

Primary bus (300)
Memory repeater hub (320)
Secondary and tertiary buses (321,322)
pp; 15 DwgNo 3/8

Title Terms: MEMORY; MODULE; COMPUTER; SYSTEM; MEMORY; REPEATER; HUB; CONNECT; PRIMARY; SECONDARY; TERTIARY; BUS
Derwent Class: T01
International Patent Class (Main): G06F-012/00; G06F-013/00
File Segment: EPI

3/5/28 (Item 23 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014592307 **Image available**
WPI Acc No: 2002-413011/200244
XRPX Acc No: N02-324497
Signals routing method in PCB, involves matching distances of connection between vias and respective land pads connected to corresponding contact and component
Patent Assignee: INTEL CORP (ITLC)
Inventor: HORINE B D; **LEDDIGE M W**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6353539	B1	20020305	US 98120517	A	19980721	200244	B

Priority Applications (No Type Date): US 98120517 A 19980721
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6353539	B1		13	H05K-007/02	

Abstract (Basic): US 6353539 B1
NOVELTY - The pitches of traces (316) carrying respective signals from specific vias on one side of PCB to the other side, are matched. Distances of connections between vias and respective land pads connected to corresponding contact and components, are matched.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) Printed circuit board;
(b) Memory module;
(c) Computer system.
USE - For routing signals between components in PCB (claimed) of memory module (claimed) used in manufacturing computer system (claimed).
ADVANTAGE - The cost is reduced by avoiding the manufacturing of mirrored packages of the components. Distance of connection is matched by adding stub length to shorter connections.
DESCRIPTION OF DRAWING(S) - The figure shows a memory module.
Traces (316)
pp; 13 DwgNo 3/7
Title Terms: SIGNAL; ROUTE; METHOD; PCB; MATCH; DISTANCE; CONNECT; VIAS; RESPECTIVE; LAND; PAD; CONNECT; CORRESPOND; CONTACT; COMPONENT
Derwent Class: T01; V04
International Patent Class (Main): H05K-007/02
File Segment: EPI

3/5/29 (Item 24 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013725669 **Image available**
WPI Acc No: 2001-209899/200121
XRPX Acc No: N01-149843
Multimedia memory in computer system, includes memory devices serially connected between electrical connectors which are coupled to last memory device on memory modules
Patent Assignee: INTEL CORP (ITLC)
Inventor: HORINE B D; **LEDDIGE M W**

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6144576	A	20001107	US 98136797	A	19980819	200121	B

Priority Applications (No Type Date): US 98136797 A 19980819
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6144576	A		17	G11C-005/06	

Abstract (Basic): US 6144576 A

NOVELTY - The memory modules (210,211) have electrical connectors (310,320) to receive the signals which are serially routed to electrical connectors (311,321) through memory units (340,341). The memory units are serially connected between the electrical connectors on the memory modules. The electrical connectors (311,321) are coupled to last memory unit on memory modules.

DETAILED DESCRIPTION - The socket connectors (220,221) routes memory bus signals to electrical connectors (310,320), and routes-off the signals to electrical connectors (311,321) on memory modules (210,211).

INDEPENDENT CLAIMS are also included for the following:

(a) computer system;

(b) memory bus signals routing method

USE - In computer system.

ADVANTAGE - provides reliable and consistent data storage and quick responses to read and write request of processors and input-output devices.

DESCRIPTION OF DRAWING(S) - The figure shows bus routing and wiring topology for memory.

Memory modules (210,211)

Socket connectors (220,221)

Electrical connectors (310,311,320,321)

Memory units (340,341)

pp; 17 DwgNo 3/9

Title Terms: MEMORY; COMPUTER; SYSTEM; MEMORY; DEVICE; SERIAL; CONNECT; ELECTRIC; CONNECT; COUPLE; LAST; MEMORY; DEVICE; MEMORY; MODULE
Derwent Class: T01; U14
International Patent Class (Main): G11C-005/06
File Segment: EPI

3/5/30 (Item 25 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012652243 **Image available**
WPI Acc No: 1999-458348/199938
XRPX Acc No: N99-342853

Vertical package for integrated circuits (ICs)

Patent Assignee: INTEL CORP (ITLC)
Inventor: HOLMAN T J; **LEDDIGE M W**
Number of Countries: 085 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9935686	A1	19990715	WO 98US27517	A	19981221	199938	B
AU 9919463	A	19990726	AU 9919463	A	19981221	199952	
US 6005776	A	19991221	US 982775	A	19980105	200006	
EP 1051748	A1	20001115	EP 98964295	A	19981221	200059	
			WO 98US27517	A	19981221		
TW 425685	A	20010311	TW 99100001	A	19990104	200143	

Priority Applications (No Type Date): US 982775 A 19980105
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9935686	A1	E	23	H01L-023/02	

Designated States (National): AL AM AT AZ BA BB BG BR BY CA CH CN CU CZ

DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK
LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ
TM TR TT UA UG US UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR
IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

AU	9919463	A	H01L-023/02	Based on patent WO 9935686
US	6005776	A	H05K-001/16	
EP	1051748	A1 E	H01L-023/02	Based on patent WO 9935686
		Designated States (Regional): DE FR GB		
TW	425685	A	H01L-023/522	

Abstract (Basic): WO 9935686 A1

NOVELTY - The package includes several connection leads. An integrated circuit die contained in the package is generally situated along a vertical plane. An interconnect is capable of transferring information between the connection leads and the integrated circuit die. The interconnect has a first segment perpendicular to the vertical plane and connected to the connection leads. A second segment in parallel to the vertical plane is connected to the integrated circuit die.

USE - The package is used for e.g. dynamic random access memory (DRAM) etc.

ADVANTAGE - The package allows optimal memory density and operating speed.

DESCRIPTION OF DRAWING(S) - The drawing shows a vertical memory module for RDRAM (Rambus DRAM (RTM)).

pp; 23 DwgNo 11/11

Title Terms: VERTICAL; PACKAGE; INTEGRATE; CIRCUIT
Derwent Class: U11; V04
International Patent Class (Main): H01L-023/02; H01L-023/522; H05K-001/16
International Patent Class (Additional): H01L-023/043; H01L-023/047; H01L-023/053; H01L-023/057; H01L-023/12; H01L-023/488; H05K-001/11; H05K-001/14; H05K-001/18; H05K-007/02; H05K-007/06; H05K-007/20
File Segment: EPI

3/5/31 (Item 26 from file: 350)

012506982 **Image available**
WPI Acc No: 1999-313087/199926
XRPX Acc No: N99-233864

Connector e.g. for coupling high frequency signals between devices such as microprocessors

Patent Assignee: INTEL CORP (ITLC)
Inventor: **LEDDIGE M** ; SPRIETSMA J
Number of Countries: 083 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9922552	A1	19990506	WO 98US17397	A	19980820	199926	B
AU 9891134	A	19990517	AU 9891134	A	19980820	199939	
EP 1029431	A1	20000823	EP 98943307	A	19980820	200041	
			WO 98US17397	A	19980820		
US 6111205	A	20000829	US 97959244	A	19971028	200043	
TW 389008	A	20000501	TW 98116564	A	19981006	200062	

Priority Applications (No Type Date): US 97959244 A 19971028
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9922552	A1	E	23	H05K-007/02	

Designated States (National): AL AM AT AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

AU 9891134 A H05K-007/02 Based on patent WO 9922552
EP 1029431 A1 E H05K-007/02 Based on patent WO 9922552
Designated States (Regional): DE FR GB
US 6111205 A H05K-001/14
TW 389008 A H01R-023/68

Abstract (Basic): WO 9922552 A1

NOVELTY - The connector has an array of vias formed on a substrate surface for coupling a reference voltage to the surface. Signal traces couple signal between the devices, the signal traces are routed through the vias. Reference voltage traces alternating with the signal traces and coupled to the vias to provide an array of voltage reference structures extending between the devices, each reference structure has a width which varies to provide a constant separation between each signal trace and each reference voltage structure adjacent to the signal trace.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a connector for coupling high frequency signal across a surface of a substrate, and a connector for high frequency signals.

USE - For coupling high frequency signals between devices such as microprocessors.

ADVANTAGE - Provides coupling for high frequency signals on tightly configured signal traces with reduced signal degradation.

DESCRIPTION OF DRAWING(S) - The figure shows a diagram of a high frequency signal connector in accordance with the invention.

pp; 23 DwgNo 4a/4

Title Terms: CONNECT; COUPLE; HIGH; FREQUENCY; SIGNAL; DEVICE; MICROPROCESSOR
Derwent Class: T01; V04
International Patent Class (Main): H01R-023/68; H05K-001/14; H05K-007/02
File Segment: EPI

3/5/32 (Item 27 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010458911 **Image available**
WPI Acc No: 1995-360230/199547
XRAM Acc No: C95-157524
XRPX Acc No: N95-267762

Appts. for attaching optical transducing subassembly to electronics circuit board - has heat spreader card mounting subassembly and flexible cable between card and board providing thermal insulation

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: BLOCK T R; GAIO D P; GUENTHER C J; KARST D L; KIDD T D; **LEDDIGE M W**
Number of Countries: 005 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 678765	A1	19951025	EP 95480010	A	19950221	199547	B
JP 7294783	A	19951110	JP 9583704	A	19950410	199603	
US 5513073	A	19960430	US 94228972	A	19940418	199623	

Priority Applications (No Type Date): US 94228972 A 19940418
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 678765	A1	E	9	G02B-006/42	
Designated States (Regional): DE FR GB					
JP 7294783	A		1	G02B-006/42	
US 5513073	A		8	H05K-007/20	

Abstract (Basic): EP 678765 A

Appts. for attaching an optical transducing subassembly (14) to an electronics circuit board (16) comprises a heat spreader card (12) on which the subassembly is mounted perpendicular to its surface, and a flexible cable (22) connecting the card to the board.

Pref. the cable has a polyimide matrix to thermally insulate the card and board.

USE - For interfacing between a data processing system and an optical data channel.

ADVANTAGE - Provides thermal and mechanical isolation of optical and electronic components while permitting close impedance matching.

Dwg.2/4

Title Terms: APPARATUS; ATTACH; OPTICAL; TRANSDUCER; SUBASSEMBLY; ELECTRONIC; CIRCUIT; BOARD; HEAT; SPREAD; CARD; MOUNT; SUBASSEMBLY; FLEXIBLE; CABLE; CARD; BOARD; THERMAL; INSULATE

Derwent Class: A89; P81; V07

International Patent Class (Main): G02B-006/42; H05K-007/20

International Patent Class (Additional): H01R-009/07; H01R-009/09

File Segment: CPI; EPI; EngPI

3/5/33 (Item 28 from file: 350)

DIALOG(R)File 350:Derwent WPIX

007093772

WPI Acc No: 1987-093769/198713

Related WPI Acc No: 1992-123447; 1993-026997; 1993-404066; 1994-199582; 1995-060383; 1995-060384; 1995-060385; 1995-074151; 1996-200349

XRAM Acc No: C87-039057

New amino-substd. steroid(s) - useful as therapeutic agents for numerous conditions with lower side effects than usual glucocorticoid(s)

Patent Assignee: UPJOHN CO (UPJO); MCCALL J M (MCCA-I)

Inventor: AYER D E; JACOBSEN E J; KARNES H A; MCCALL J M; PALMER J R; VAN DOORNIK F J; VAN DOORICK F J; AYER D; JACOBSEN E; **MCCALL J** ; VANDOORNIK F; VANDOORNIK F J

Number of Countries: 025 Number of Patents: 023

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8701706	A	19870326	WO 86US1797	A	19860828	198713	B
AU 8663356	A	19870407				198726	
NO 8701930	A	19870720				198734	
EP 238545	A	19870930	EP 86905605	A	19860828	198739	
DK 8702375	A	19870511				198804	
FI 8702107	A	19870512				198806	
EP 263213	A	19880413	EP 86307808	A	19861009	198815	
ZA 8606097	A	19880215	ZA 866097	A	19860613	198817	
JP 63500868	W	19880331	JP 86504810	A	19860828	198819	
CN 8606226	A	19870318				198823	
AU 8940806	A	19891207				199004	
AU 8940807	A	19891207				199004	
IL 79702	A	19920216	IL 79702	A	19860812	199220	
IL 98007	A	19920216	IL 98007	A	19860812	199220	
JP 93035158	B	19930525	JP 86504810	A	19860828	199323	
			WO 86US1797	A	19860828		
NO 176762	B	19950213	WO 86US1797	A	19860828	199511	
			NO 871930	A	19870511		
FI 94417	B	19950531	WO 86US1797	A	19860828	199527	
			FI 872107	A	19870512		
EP 263213	B1	19950906	EP 86307808	A	19861009	199540	N
EP 238545	B1	19951115	EP 86905605	A	19860828	199550	
			WO 86US1797	A	19860828		
DE 3650440	G	19951221	DE 3650440	A	19860828	199605	
			EP 86905605	A	19860828		
			WO 86US1797	A	19860828		
ES 2078890	T3	19960101	EP 86307808	A	19861009	199608	N
JP 2768864	B2	19980625	JP 86504810	A	19860828	199830	
			JP 928428	A	19860828		
MX 185563	B	19970811	MX 923466	A	19920626	199847	

Priority Applications (No Type Date): US 86888231 A 19860729; US 85775204 A 19850912; US 85811058 A 19851219; US 86877287 A 19860623; EP 86905605 A

19860828
Cited Patents: 5.Jnl.Ref; DE 1087598; FR 1413722; GB 1345640; GB 1390014; GB 954146; No-SR.Pub; US 2665274; US 3144446; US 3558608

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8701706	A	E			
Designated States (National): AU DK FI JP KR NO SU US					
Designated States (Regional): AT BE CH DE FR GB IT LU NL SE					
EP 238545	A	E			
Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE					
EP 263213	A	E			
Designated States (Regional): AT ES GR					
IL 98007	A			C07D-213/62	Div ex patent IL 79702
JP 93035158	B			C07J-043/00	Based on patent JP 63500868 Based on patent WO 8701706
NO 176762	B			C07J-041/00	Previous Publ. patent NO 8701930
FI 94417	B			C07J-041/00	Previous Publ. patent FI 8702107
EP 263213	B1	E	130	C07J-041/00	
Designated States (Regional): ES GR					
EP 238545	B1	E	129	C07J-041/00	Based on patent WO 8701706
Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE					
DE 3650440	G			C07J-041/00	Based on patent EP 238545 Based on patent WO 8701706
ES 2078890	T3			C07J-041/00	Based on patent EP 263213
JP 2768864	B2		70	C07D-213/65	Div ex application JP 86504810 Previous Publ. patent JP 5112597
IL 79702	A			C07J-041/00	
MX 185563	B			C07J-043/000	

Abstract (Basic): WO 8701706 A

C07j 5/00, 7/00 Amino-substd. steroids of formula (I) and their salts, hydratand solvates are new. (A-1) R6=alpha R61:beta R62; R10=alpha R101:beta R102; R7=alpha H:beta H; one of R61 and R62=H; and the other=H, F or 1-3C alkyl; R102=Me; R101+R5=-(CH2)2-C(=R33)-CH=-CH=CH-CO-CH=; R33==O or alpha H:beta OR34 or alpha OR34:beta H; R34=H, PO(OH)2, COMe, COEt, COPh, COOMe or COOEt; (A-2) R5=alpha R53:beta R54; R6=alpha R63:beta R64; R10=alpha R103:beta R104; R7=alpha H:beta H; one of R63 and R64=H; and the other with one of R63 and R64 forms a second bond between C5 and C6; R104=Me; R103 and the other of R53 and R54=-(CH2)2-CH(OH)-CH2- or -(CH2)2-CH(OP(O)(OH)2)-CH2-; (A-3) R10+R5==CH-CH=C(OR3)-CH=; R3=H, PO(OH)2, 1-3C alkyl, CHO, 2-4C alkanoyl or benzyl; R6=alpha R65:beta R66; one of R65 and R66=H; and the other=H, F or 1-3C alkyl; R7=alpha H:beta H; (A-4) R5=alpha R54:beta R58; R6=alpha R67:beta R68; R7=alpha H:beta H; R10=alpha R107:beta R108; one of R57 and R58=H; and R107 and the other=-(CH2)2-C(=R33)-CH2- etc. R108=Me; etc.

USE/ADVANTAGE - (I) and (II) are useful for treating various medical conditions in humans and animals. In humans they are useful in treating spinal trauma, head injury, subarachnoid haemorrhage, cerebral vasospasm, ischaemic stroke, excessive mucous secretion, etc., inflammatory diseases e.g. arthritis, nephrotic syndrome, systemic lapus erythematosis, allergic reactions, atherosclerosis. Some cpds. are esp. useful for burn healing, wound healing and post MI heart recovery, and for preventing damage after cardiopulmonary resuscitation, neurological and cardiovascular surgery and cardiac (I) may be used in humans and animals for treating conditions where glucocorticoids are normally used, but without Dose is 0.05-100mg/kg daily 1-4

Title Terms: NEW; AMINO; SUBSTITUTE; STEROID; USEFUL; THERAPEUTIC; AGENT; NUMEROUS; CONDITION; LOWER; SIDE; EFFECT; USUAL; GLUCOCORTICOID

Derwent Class: B01; B03; C02; C03

International Patent Class (Main): C07D-213/62; C07D-213/65; C07J-041/00; C07J-043/00; C07J-043/000

International Patent Class (Additional): A61K-031/056; A61K-031/56; A61K-031/58; C07C-093/14; C07C-217/54; C07D-213/02; C07D-213/74; C07D-239/24; C07D-239/48; C07D-239/50; C07D-245/08; C07D-249/08; C07D-249/14; C07D-251/12; C07D-251/54; C07D-251/70; C07D-253/06;

C07D-295/12; C07D-295/182; C07D-307/68; C07D-333/52; C07D-333/66; C07D-401/04; C07D-401/14; C07D-405/06; C07D-409/06; C07D-413/14; C07J-005/00; C07J-007/00
File Segment: CPI

3/5/34 (Item 29 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004843166
WPI Acc No: 1986-346507/198652
XRAM Acc No: C87-000025
Antiarrhythmic method using N-aminocycloalkyl-aroylamide cpds. - e.g. trans-para-bromo-N-2-aminocyclohexyl-benzamide
Patent Assignee: MCCALL J M (MCCA-I); UPJOHN CO (UPJO)
Inventor: GIBSON K J; KANE P F; LUDERER J R; **MCCALL J**
Number of Countries: 014 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8607257	A	19861218	WO 86US1111	A	19860522	198652	B
EP 224566	A	19870610	EP 86903872	A	19860522	198723	
EP 263208	A	19880413	EP 86307770	A	19861008	198815	
JP 63500796	W	19880324				198818	

Priority Applications (No Type Date): US 85742248 A 19850607; EP 86903872 A 19860522
Cited Patents: No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8607257	A	E	32		
Designated States (National): JP					
Designated States (Regional): AT BE CH DE FR GB IT LU NL SE					
EP 224566	A	E			
Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE					
EP 263208	A	E			
Designated States (Regional): AT ES GR					

Abstract (Basic): WO 8607257 A
Antiarrhythmic method comprises admin. of an aminocycloalkyl amide of formula (I) or pharmaceutically acceptable salt; where A=-(CH2)q-, -CHMe or a bond; q is 1-4; E=O or S; Q=1-or 2-naphthyl or -C6H3XY; X and Y each=H, F, Cl, Br, CN, SO3H, methanesulphonyl, formyl, acetyl, propionyl, OH, CF3, 1-3C alkyl, 1-3C alkoxy, phenyl, NH2, mono- or di(1-3C alkyl) amino, NO2, N3, 1-3C alkoxycarbonyl, 1-3C alkanoyloxy, -NH-CO-R8, benzoyl, HCOO- or -C(Rk)(Rl)-C(Rm)=C(Rn)(Ro); R8=H or 1-2C alkyl; Rk-o each=H or alkyl with the proviso that they contain max. 3C in total; R=H or 1-3C alkyl; R1=H, 1-3C alkyl or -C(Rk)(Rl)-C(Rm) C(Rn)(Ro); R2=H, 1-10C alkyl, 3-12C cycloalkyl, 4-8C cycloalkyl-1-4C alkylene, CF3CH2-, -C(Rk)(Rl)-C(Rm)=C(Rn)(Ro), -CH2-1-4C hydroxyalkyl, 2-phenylethyl, 3-phenylpropyl, 2-furylmethyl or 2-thienylmethyl; or NR1R2=a heterocycle of formula (II), (III) or (IV), pyrrolyl, 3-pyrrolin-1-yl, 3-azabicyclo(3.1.0)hexan-3-yl or 3-azabicyclo(3.2.0)heptan-3-yl; b=1 or 2; G=OH or 1-3C alkyl, alkoxy or alkanoyloxy; J and J' each=H, OH or 1-3C alkyl, alkoxy or alkanoyloxy with the proviso that J or J' must be H; x=0 or 1; y=2, 3 or 4; R10=H or 1-3C alkyl; R3=H, OH, 1-3C alkoxy, R9-CO-O-, mercapto or 1-3C alkylthio; R9=H or 1-3C alkyl; R4=H or 1-3C alkoxy or alkylthio; or R3 and R4 together=-Z-(CH2)m-, -CH2-Z-(CH2)r-, =E, -E-(2-5C alkylene)-E-, =N-OH or =N-OAc, with the proviso that when R3=H, R4 may form a C-C double bond with an adjacent unsubstd. C atom; Z=O, S or -SO-; m=3 or 4; r=2 or 3; a=0 or 1; n=0 or 1-9; and p=0 or 1-9
USE - Method is useful for preventing or reducing the no., frequency or severity of arrhythmic events, palpitations, faitings or syncope. (32pp Dwg.No.0/0)
Title Terms: ANTIARRHYTHMIC; METHOD; N; AMINO; CYCLO; ALKYL; AROYL; AMIDE; COMPOUND; TRANS; PARA; BROMO; N; AMINO; CYCLO; HEXYL; BENZAMIDE

Derwent Class: B03; B05
International Patent Class (Additional): A61K-031/16
File Segment: CPI